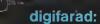


54 October 1979 U.K. 55 p. U.S.A. Can. \$1.75

Ip

gate dip
a modern grid
dip meter

touch luning for F.M. tuners



capacitance meter with digital readout.

page 10-06

Construction of the touch tuning circuit requires a bit of handiwork with a fret saw. The printed circuit board consists of three sections; once separated, the two smaller sections are mounted perpendicularly to the main board to form a compact module.



page 10-22

The gate dipper is a useful little device that can be used to determine the resonant frequency of tuned circuits. Basically, it is the modern equivalent of the old grid-dip meter.



page 10-26

The 'heart' of the strain gauge is the 'stress absorber', which consists of a sheet of suitable metal onto which a bridge configuration of four electric resistance strain sensors are bonded.



page 10-28

'I played TV games . . . is a description of the TV games computer, written by a novice and for novices! One thing has become guite clear: with a little practice. even fairly sophisticated programs can be designed.



selektor	1	0.

touch tuning 10.06 An important selling point of modern stereo tuners is the number of preset stations which can be selected. However for the home constructor, this is often a leature which must regrettably be foregone, being regarded in many designs as something of a luxury. The circuit described is intended to remedy that situation, by providing for up to 9 touch controlled preset stations. The only restriction is that the receiver

attery save	٠.,			,	,						٠				10	-0	9

10-10 impedanca bridga It is often very useful to be able to match the values of capacitors and resistors and the only quick, affective way to do this is by using an impadence bridge. The circuit described is quite adequate for this purpose and it is also capable of massuring resistances between 100 Ω and 1 M and capacitances between 100 pF and 1 μ F

10.12 Good news for SC/MP liens two new records have been added to the ESS range. One contains the complete NIBL-E program; the other includes some games, a "running script

		e letter prog		given here.	DOTTIE	
digital re	ev cour	ter in o	orie)			10-1

digifarad (J. Guther) 10.18 Given the fect that many types of capacitor - especially electrolytics - have a wide tolerance (20% is fairly common), it is often desirable to be able to measure capacitances both

quickly and with a reasonable degree of accuracy. Of course a capacitance mater also anables one to measure the value of those piles of unmarked depetitors which and up at the bottom of one's junk box, or to test 'suspect' depetitors for potential laults - in short it represents a useful addition to the test gear of any constructor.

snort-interval light switch	10.70
p.c.b. for variabla fuzz box	10.20
gate-dipper	10-22

Tuning resonant circuits in high frequency equipment normally requires feirly expansive test gear which not every hobbyest can efford. However there is a reasonably cheep alternative everlable, namely a gets dipper, which allows the

simply and quickly	
strain gauge (W. v. Oreume) There are leve projects which have not formed the subject of a stricle in Elaktor at one time or another, however a stricle gauge falls into their category. This in itself is perhaps slightly surprising, since there are a number of possible application for such a device — a training aid for 'strength's porce'.	f n /

measuring loads on cables, esc. or simple weighing purposes.	
I played TV games	10.28
Writing your own programs for the TV games computer is	
fairly easy, provided you know the basic principles. The most	
important instructions are discussed this month, with some	

programmable sequencer (C. Voss)	10.38
nissing link	10-41
nerket	10-41
dvertisers index	UK-30



Volume 5

Number 10

other countries

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ABC

What is a TUN? What is 10 n? What is the EPS service?

What is the TD service? What is a missing link? Semiconductor types

Very often, a lerge number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

 741' stend for μA741, LM741, MC641, MIC741, RM741, SN72741, atc.

a 'TUP' or 'TUN' (Transistor, Universel, PNP or NPN respect ively) stand for any low frequency silicon transistor that meets the following specifi-Cations:

20 V UCEO, max IC. max 100 mA hfe, min 100 100 mW Ptot, max fT, min LOO MHz Some 'TUN's are BC107, BC10B

and BC109 lamilies; 2N3856A. 2N3859, 2N3860, 2N3904, 2N3947, 2N4124, Some 'TUP's ere: BC177 and BC17B femilies. BC179 family with the possible exeption of BC159 and BC179. 2N2412, 2N3251, 2N3906, 2N4126, 2N4291,

a 'DUS' or 'DUG' (Diode Univerest. Siticon or Germanium respectively) stands for any diode that meets the following specifications.

	DUS	DUG
UR, max	25V	20V
IF, max	100mA	35mA
IR. max	1µA	100 µA
Ptot, max	250mW	250mW
CD, max	5pF	10pF

Some 'DUS's are: BA127 BA217 BA218, BA221, BA222, BA317, BA318, BAX13, BAY61, 1N914 1N414B Some 'DUG's ere DA85, OA91, OA95 AA116

a 'BC1078', 'BC2378', 'BC5478' all refer to the esma 'femily' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC107 (-8, -9) families: BC107 (48, 9) RC147 (48, 9) BC207 (48, 9), BC237 (48, 9), BC237 (48, 9), BC317 (48, 9), BC317 (48, 9), BC317 (48, 9), BC182 (3, 4), BC382 (3, 4), BC437 (48, 9), BC414

BC177 (-8, -9) families: 8C177 (-8, -9) annines 8C177 (-8, -9) 8C157 (-8, -9), 8C204 (-5, -8), 8C307 (-8, -9), 8C320 (-1, -2), 8C350 (-1, -2), 8C527 (-8, -9), 8C251 (-2, -3), 8C212 (-3, -4), 8C512 (-3, -4), 8C261 (-2, -3), 8C416.

Resistor and capacitor values When giving component values, decimal points and large numbers

of zeros are evolded wherever able. The decimal point is usually replaced by one of the following abbreviations: D

10 (pico-) 10.3 (nano-) = 10-6 (micro-) = 10-1 (milli-) = (kilo-) 103

M (mege-) = 104 (giga-l 10" A few exemples Resistance value 2k7 2700 Ω.

Resistance value 470 470 Ω Capecitance value 4p7: 4 7 pF, or 0.000 000 000 004 7 F Capacitance value 10n, this is the international way of writing 10,000 pF or .01 µF, since 1 n is

10" farads or 1000 pF Resistors ere % Watt 5% cerbon types, unless otherwies specified. The DC working voltage of capecitors (other then electrolytical is normally assumed to be at least 60 V. As a rule of thumb, a esta valua is usually approxi-

mately twice the DC supply voltage Test voltages
The DC test voltages shown are

measured with a 20 kΩ/V instrument, unless otherwise specified.

The international letter symbol 'U' for voltage is often used Insteed of the ambiguous "V 'V' is normally reserved for 'volts'. For Instance Ub = 10 V, not Vb = 10 V

Mains voltages

No mains (power line) voltage ere listed in Elektor circuits, It is assumed that our readers know what voltage is standard in their part of the world!

Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modific cation may be required

Technical services to readers a EPS esrvice Many Elektor articles include a lay-out for a printed circuit board. Some - but not all - of these boards are available ready-exched and predrilled. The 'EPS prim service list' in the current issue always gives a complate list of evalleble boarde

a Technical gueries Members of the technical staff era available to answer technical queries (relating to articles published in Elaktor by telephone on Mondays from 13 30 to 16 45 Letters with tachnical gueries should be

addressed to: Dept. TD. Please enclose a stamped, self addressed envalope: reeders outside U.K. please enclose an IRC instead of

Missing link Any important modifications to, additions to. improvements on or corrections in Elektor circuits are generally listed under the heading 'Missing Link' at the earliest opportunity.

New home-video standard from Philips

8 hours of TV from one cassette

The latest Phillips and Grundig top-hit in the home-video field, the Video-2000 system, has received world-wide attention. One cassette, containing about 1000 feet of 1/2 inch taps, can be used to record eight hours of colour TV. One cassetta costs about £ 20, so that one hour of TV program costs just over £ 2 to record, By way of comparison, the first colour video recorder used well over £ 20 of tape per hour. The picture quality hasn't suffered by this drastic cost reduction. All in all, it's not just another step forward - it's a giant leap! Obviously, Philips and Grundig hope that the new video cassette will be accepted as an international standard. and that it will prove the same longterm success as its predecessor; the compact audio cassette.

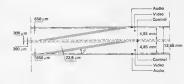
The Philips recorder, designed around this new cassetta, is a beautiful piece of modern technology.

The first obvjous difference between the Video 2000 system and older Philips systems (and JVC's VMS and Sony's highly praised stemand) is the neirow tape-track used. Until now, Seindo Grundig use less than half – the Seindo fraction, since the cassite can be "turned over." It is used in the same way as the sudio compact cassette — the only difference is that it is used to record television programs!

The new cassette can not be used on older video recorders, like the N1700. That particular machine will be goling out of production in the second half of 1980; suitable cassettes will, however, remain available for some time to come. A new video recorder, the VR2020, is designed to use the new cassetts. The price is expected to be about 30% more than the of the N1700 — and the think of the N1700 — and the think of the N1700 — and the included in the new machine, and these deserves one further explanation.

Use of the tape

Before discussing the recorder itself, it is a good idea to take a look at the way in which it writes the program material on tape. Figure 1 shows where the information is written on the tape.



Since the tape can be "turned over", the upper and lower half of this "taps map" are mirror images. Starting from the outside, the first 650 µm ers used for a (mono) audio track. At a later date, if stereo sound ever gets off the ground for television broadcasting, this area can be divided into two 250 µm tracks with a 150 µm as 150 µ

The next 488 mm wide section is received for the video signal. This is recorded in a single track, like the suicil signal, as in most video recorders, nerrow (22.6 µm wide) tracks are recorded at slight angle in this section. In this particular case, the video tracks are angled at 3° with raspect to the taps "asis" for clarity, an angle closer to 30° is used in figure 1. . The final section of tape before reaching the contreasured of tape the contract of the property of of the

All these sections are repeated on the other side of the centre line, for what is celled (in analogy with gramophone records) 'the other side of the tape'.



Video recording

Which is what the whole exercise is about... The video signels to be recorded run up to fairly high frequencies (approximately 4.8 MHz). In any type of recording, the 'detail' that can be written depends on how coarse to the writing implement is. In a tage recorder, the recording implement is the tape head; its 'gap width' determines the detail that it can write on the tape.

on the tepe. However, the 'space' required to record one period of a 4.8 MHz signal on tape depends on the speed with which the tape runs past the heads. The higher the speed, the longer a single period will be



ARRE 1

stretched on the tapa. If the tapa runs relatively slowly, a larger number of periods could theoretically be recorded on a small section of tape; however, tha tape head is too 'blunt' to make this a feesible proposition. The result would be poor picture quality. Somehow, the speed of the tape relative to the head must be increased until the picture quality leaves little to be desired. If the tape is run at high speed past a stationary head, the picture quality can be quite good - but the recorder will 'eat' tapa, both in feet of tape required per minute end in life expectancy of the tape . . For this reason, it has become standard practice in video recorders to use a rotating head drum, incorporating two or more heads. This drum revolves at high speed, so that the heads move at high speed past the tape, even if the latter is trensported relatively slowly. The head drum is mounted at a slight angle with respect to the tape and vary narrow video tracks are used, so that a fairly slow tape transport suffices to move the tape up sufficiently to write the next diagonal track adjacent to its

predecessor. All this may seem rather complicated. but it is basically similar to typing. Even if you type a lot of letters, it takes a while to fill the page - certainly if you use the minimum line spacing, so that each new line practically touches the one above. Something similar occurs in a video recorder; the main difference being that the tape is moved slowly and constantly, instead of jumping up 'one line at a time' like the paper in the typewriter. If you can visualise the paper moving up at a constant speed, so that it has just moved up one line by the time you start to type a new line (so that the lines slope down slightly), you have the principle of the video recorder.

Figure 2 illustrates how this system operates in practice. Two heads are mounted on the drum, and the latter is mounted at a slight angle with respect to the tape. As the tape is transported at a speed of 2.44 cm/s (just less than 1 inch/second, or about half the speed of an audio cassette recorder!), diagonal tracks are written on it by the heads on the upper half of the drum. The lower half of the drum runs at a much lower speed, and takes care of the tape transport - it operates as a large diamater 'capstan'. The diameter of the drum is 65 mm and the upper half rotates at 25 revs per second, so that the two heads (K1 and K2) move at 5.08 m/s - or just under 17 ft. par second! The tape is 'wrapped around' half tha circumference of the drum, so that as one head leaves the tape the other just starts to write on it. It will now be apparant how the tracks are recorded. The tape is almost stationary with raspect to the upper half of the drum, One head can therefore record a track length equal to approximately half the diameter of the drum - vary roughly, 100 mm or 3/8",

We said that the tape is almost stationary with respect to the heed. To be mora precise, that tape is transported over 22.6 µm as one full track is recorded. When the second head 'hits the track' he tape his moved up just far enough to enable this head to record its track overlaping. The final result is allowed overlaping. The final result is allowed of disponal tracks, as illustrated in figures 1 and 2.

A separate, stationary head is used to record the audio signal. This 'sound track' is located at the outer edge of tha tape, as illustrated in figure 1. The erase heads are also stationary.

Vartical positioning of the video heads

With the extremely narrow video tracks written diagonally on the taps, positioning of the video heads during playback is obviously highly critical. Some way must be found to move the heads slightly until they are centred exactly on the corresponding tracks. A most intriguing solution has been found, The video heads are both mounted on a little piece of piezo-ceramic material. This is the material used in no-battery electric lighters: when it is compressed, a voltage appears across the ends, sufficient to draw a spark. However, it also works the other way: if a voltage is applied across the ends of the material. its shape will vary! The so-called PXE is used in this way in the video recorder.





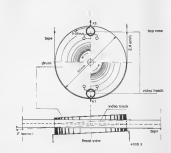
By varying the voltage applied to it, the height of the heeds can be adjusted.

Dynamic Track Following

It's all very well being able to vary the position of the heads, but first a control voltage must be derived in some way, Figura 3 again shows four video tracks with an exagerated engle (the true angle being only 3°). Track 15' is written first, then 14 is recorded, and so on, And this is where it gets complicated. Tracks 12' and 13' are written by video head two; tracks 14' and 11' are recorded by haad one. Simultaneously with the video signal, a 'pilot tone' is recorded on



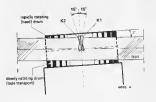
aach track. Each haad records two different (relatively low frequency) pilot tones afternately. Track (2 contains a 117 kHz pilot tone, recorded by K2 (video haad 2); track f4, written by K1, includes a 164 kHz pilot tone; on track f3, the pilot tone frequency is 149 kHz; finally. the pilot tone no track f1 is



3

f1 = K1 pilot tone 102 kHz 12 = K2 pilot tone 117 kHz 14 = K1 pilot tone : 164 kHz

13 = K2 pilot tone : 149 kHz



102 kHz. This cycle is repeated for the next set of four tracks, and so on.

During playback, the pilot tones are retrieved together with the video signal. If the corresponding head (K1) is correctly positioned, a clean 164 kHz tone will be retrieved from track f4. However, if the head is slightly high, some of the 149 kHz signal on track f3 will be mixed with this 164 kHz signal, producing e 15 kHz beet signal; if the head is low, a 47 kHz beat signal will appear (164 kHz (f4) - 117 kHz (f2) = 47 kHz). For the other head (K2), the opposite is true: if it is too high, a 47 kHz signal is produced; a 15 kHz beat signal corresponds to 'too low'.

The amplitude of the beat signals is used as a basis for the 'head height' control signal.

Azimuth

The video heads are mounted in the haad drum at a relative angle of 30°. With respect to the tapa, head one is mounted et $90^{\circ} - 15^{\circ} - 3^{\circ} = 72^{\circ}$, head two is mounted at $90^{\circ} + 15^{\circ} - 3^{\circ} = 102^{\circ}$. This is illustrated in figure 4, whara both haads are shown simultaneously with respect to the tape. There is good reason for the relative angle between the two heads.





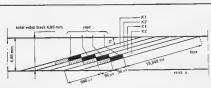
As audio recorder enthusiasts will know, if a playback head is tilted slightly with respect to the recorded tape track, the high frequency response is drastically reduced. Correct 'azimuth' setting is essential for high quelity playback. In this video recorder, the result is that a track originally recorded by K1 will only ba 'read' by K2 with a severely reduced high-frequency response. In practical terms, this means that K2 will only 'see' frequencies Up to a few hundrad kilohertz on K1's tracks - K2 will reproduce K1's pilot tones, but it will not reproduce the video signel! Cunning . . .

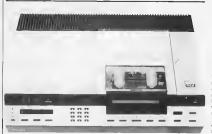
Head positioning during recording

During recording, accurate positioning of the heads is also required, to keep the trecks up against eech other without overlap. To this end, one of the heads is fixed in en 'averege' position; the height of the other is adjusted so thet its tracks are correctly positioned. A complete TV picture consists of

625 lines, written in two 312.5 line 'frames'. Between each set of 312.5 lines, a short 'vertical blanking' intervel is required. No video signal is recorded in this interval. One complete picture (two frames) is recorded 25 times per second . . . exectly the rotation speed of the head drum! Coincidence? Don't you believe it. Each head records one frame, and two frames make one picture. Each track includes a vertical blanking interval, which can be used to record e control signal. In the VR 2020, a 223 kHz signal is recorded at this point, for 96 µs. Immediately after this, the head is switched to playback for a further 96 µs. The result of these manipulations is sketched in figure 5. Bearing in mind that the right-hand track is recorded first (the tracks themselves are racorded from lower laft to upper right, but the tepe movement is also from left to right) it will be

5





epparant that when head K1 is switched to playback ('reed') it will datect the 223 kHz tone recorded on the previous track by K2 if the latter is high. Similarly, if K2 is low it will detect the 223 kHz signal from the previous track during its own read cycle. Using this information, the height of one of the heads is adjusted until the tracks just mesh correctly

As illustrated in figure 5, 960 μs (15 lines) of video ere recorded on each track before the 223 kHz test signal. Each track tharafore contains the following sequence: first 15 lines at the end of a frame, then 96 µs worth of the test signal, than the head is switched to pleybeck for a further 96 µs, then the first 294.5 lines of the next frame. The other head now takes over on the next treck, recording the last 15 lines of the frama, and so on.

It will be obvious that some fairly fast. complicated and occurate switching is required for the VR 2020 to work . . . For this reason, the whole system works undar microprocessor control.

Other gimmicks

It may seem surprising, but the head drum is heated in the VR 2020, Among other advantages, this ensures a constant diameter, raduces the tendency of the tape to 'stick' to the heeds and reduces the wear on the heads.

If, during playbeck, both heads are found to be slightly high or if both are slightly low, the tape is shifted up or down slightly instead of adjusting the position of the heads. This is called

'Automatic Tracking'. The control voltage from a Dynamic Track Following 'discriminator' is used to control a tape servo. During recording, a constant tape speed is maintained by referring the output of a tacho ganerator to that of a crystel oscillator; during playback, tha DTF control voltage is used as a reference, so that both the tape speed and the tape position with respect to the heads is accurately maintained.

The rapidly rotating half of the head drum must also run at axactly the right speed. This is achieved by measuring the speed of the drum with a phototrensistor that gives one pulse for each rotation of the drum; the frequency of these pulses is compared with that from the tacho generator that measures the tape speed. The VR 2020 is quite easy to operate. Most of the functions are eutometed. and it is possible to 'program' it up to 16 days in advance. The cassettes for the Video 2000 system include machenical 'record locks' that can be used to protect recorded tapes from inadvertent re-use.

The future

As mentioned in the introduction, Philips and Grundig hope that this system will become an international stendard. Apperently, ITT have already decided to use the new cassette, and the German manufacturers Loewe Opta and Metz ere taking a long, hard look et it. It looks as if this system has a good chance of making the grade!

Philips Gloeilampenfabrieken. P.O.B. 523. Eindhoven, The Netherlands

Grundig AG. Kurtgartenstrasse 37 8510 Fürth/Bayern, West Germany.

Switching transistors approach 1000 V Barrier

The switch mode power supply has a number of advantages over other conventional supplies. However, their use in high power circuits has been limited by the absence of transistors with sufficiently good characteristics to meet the heavy demands placed on tham under high voltage switching conditions. An ideal switching transistor should have cheracteristics that include:

- very low VCE sat
 - very low leakage current
 - very good switching characteristics
- very good ruggedness

a good reliability

Characteristics that era difficult to obtain in high voltage high power transistors. The SGS-ATES MULTIEPITAXIAL MESA technology, which was created to overcome these problems, gives an excellent compromise between thase characteristics. In addition to this it gives the possibility of making complamentary NPN-PNP high voltage, high power transistors, a feature impossible to find in other high voltage, very high power technologies In the Multiepitaxial Mesa technology a

heavily doped N° substrate is used as e foundation onto which is epitaxially grown a normelly doped N type layer, On the N type layer is grown a second epitaxial layer of lightly doped N" type material. These two epitaxial layers form the collector of the trensistor. This type of collector construction gives extremaly good ruggedness in Es/b conditions. On top of the collector is grown a third epitexial lever which is to form the base of the trensistor (into which an No type emitter diffusion is mede). This epitaxial layer, in order to maintain the high voltage characteristics of the device whilst giving good switching times, must be of a P" type material. However, if the emitter diffusion was made into the base as it stands, problems would arise in the stability of the transistor due to the very high electric field between the P"/N" layer seen at the edge surface. Therefore an additional P* diffusion is made into the base epitaxial layer that has the effect of widening the distance between equipotential lines at the surface thus reducing the surface alectric field. The P* diffusion does not of course reduce the intrinsic high voltage characteristic of the transistor

Whilst the multiepitaxial layer construction gives e breakdown value in the order of 1000 V it is known that when (489 S) transistors ere separated by mechanical means, after diffusion, irregularities are caused on the edge of the transistor which dramatically reduce the collector/ base breakdown voltage. Obvolusly the breakdown voltage of the device as a whole is the breakdown voltage of the weekest point, in this case the edge surface between collector and base Therefore a method had to be found which would allow separation of devisithout causing surface edge irreguwithout causing surface edge irregu-

larities. The method found, whilst extremely simple in concept, has had dramatic effects in improving the collector/base breakdown characteristics. In essence the method used is to isolate each transistor on the wafer by a deep chemical edge. In this way it is possible to achieve an extremely smooth edge on the active part of the transistor in the area of the base collector junction. It is the cross section of the transistor after the deep chemical etch that gives rise to the name Mesa (after the mesas found in S.W. United States and Mexico). Tha deep chemical etch is carried out after the emitter diffusion and then, to further enhance stability and preserve surface cleanliness, glass passivation is carried out on the channel formed. The cut made to separate the transistors is then made in the innactive area between

Table 1

	BUW 34	BUW 35	BUW 36	BUW 44	BUW 45	BUW 46
	BUW 34	BOSS 32	BOW 30			
VCBO(min)	500 V	800 V	900 V	500 V	800 V	900 V
VCEQ(min)	400 V	400 V	450 V	400 V	400 V	450 V
VCE(sat)max	1.5 V	t.5 V	t.5 V	1.5 V	1.5 V	1.5 V
ton(typ)	0.2 με	0.2 µs	0.2 µs	0.2 µs	0.2 με	0 2 μs
ts(typ)	1.8 µs	1.8 µs	1.8 µs	t.8 µs	1.8 µs	1.B µs
tf(typ)	0.2 μs	0.2 με	0 2 μs	0.2 μs	0.2 μ5	0.2 μs

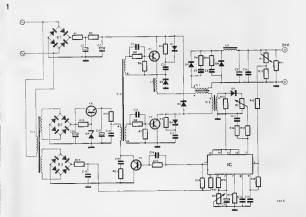
NOTE: $V_{CE(g)}$ is specified at $I_C = 5$ A, $I_B = 1$ A for BUW 34, 35,36 and $I_C = 10$ A, $I_B = 2$ A for BUW 44, 45, 46, 5w, on characteristic typified at $V_{CC} = 250$ V, $I_C = 5$ A, $I_B = I_B = 1$ A for I_C , I_C in I_C

the dice.

Using this method it has been possible to produce transistors with a Vmax as high as 900 V and with extremely good raliability and ruggedness in high voltage, high temperature conditions.

Typical electrical characteristics for transistors constructed using the multiepitaxial mesa technology are shown in table 1.

Using these transistors it has been possible to build switch mode power supplies with a performance never before possible. A typical example of these transistors in eawitch mode power supply is shown in fig. 1. This circuit, which uses two BUW 34's in the power output stage, is capable of delivering up to 400 W at 24 V or by using two BUW 45's ut 24 V.



Many FM tuners employ varicap (variable cepacitance) diodes. These re diodes which are especially designed so that their capacitance can be varied by means of a control voltage, if the varicaps are of control voltage, if the varicaps are included in en LC circuit, the resonant frequency of the latter can thus be varied by atternigh the control voltage, in most tuner designs the control or tuning voltage is derived from a stabilited supply ustage is derived from a stabilited supply to the control of the control

touch tuning

touch-controlled preset station tuning



An important selling point of modern stareo tuners is the number of preset stations which can be selected. However for the home constructor, this is often a feature which must regrettably be foregone, being regarded in many designs as something of a luxury. The circuit described here is intended to remedy that situation, by providing for up to 9 touch controlled preset stations. The only restriction is that the receiver be varient until the statement of the sta

Preset tuning can be realised by using not one potentiometer, but a number of potentiometers connected in parallel, these being selected by switches (see Figure 1), O'Ne one switch may be closed at the control of the

In the circuit described here, the besic design hes been further refined, so that using only two switches a total of 10 preset stations can be selected. By employing touch switches, the need for interlocking switch essemblies is avoided, whilst the physical construction and appearence of the switches cen be teilored to suit individuel requirements.

Circuit

For a renge of 87 to 104 MHz, the tuning voltage of most receiver must be capable of being varied from roughly 2 or 3 volts to approximately 30 volts. Thus it is clear that conventional CMOS writches cannot be used, since they are only capable of switching voltages of up to 15 V, However, as can be sen from tha circuit diagram of figure 2, CMOS buffers N1. N4 are used to form e pair of suitable touch switches.

N1 and N3 are held high via R1 and R2. When one of the sets of touch contacts is bridged, the input of the corresponding sate is pulled down to ground (logic 0). The output of the gets is thus taken high, with the result that C1 or C2 rapidly charges up and the output of the high, with the result that C1 or C2 rapidly charges up and the output of the Removing one's finger from the touch contacts takes the output of the first yate low again, cousing the corresponding capacitor to discherge slowly vie the parallal resistor. Thus each time one of

2

the touch switches is operated a togic 0 is applied to the up or down input of IC1 (synchronous decade up/down counter). This IC counts the pulses applied to its inputs when the LOAD input is high, and transfers the result in BCD form to its outputs.

Upon switch-on the LDAD input of the counter is held low via capacitor C3, so that the counter outputs are reset (i.e. elso taken low). When the 'up' touch switch is operated, the counter incoments by one, i.e. the number 1 coments to yone, i.e. the number if it is up switch is touched a second if it the up switch is touched a second time, the number 2 sepaces at the counter outputs, end so on, Touching the 'down' switch decrements the

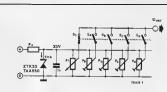


Figure 1. This errangement of potentiometers and switches represents a simple method of selecting preset stations. The only drawback is the need for an interlocking switch assembly.

30 V ⊕4 T1 ... T10 - BC 557 R12 . R29 = 10 x 100 h IC1 N1 ... N4 = IC4 = 4093 D1,D2 = DUS HP 5082-7730 a see text 79519

Figure 2. Complete circuit for preset touch tuning. Using only two touch switches a choice of 9 preset stations can be selected.

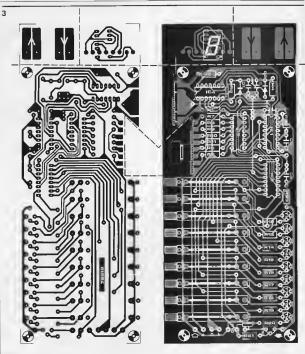


Figure 3. The printed circuit board for the touch tuning circuit, Some initial work with a frat-saw is required to separate the board into 3 sections.

perts list:

Resistors R1_R2 = 2M7 R3_R4 = 10 M R5 . R11 = 220 Ω R12 . R21_R23 = 100 k R22 = 1 M P1 . . . P9 = 20-turn preset potentiometer (Piher), 50 k or 100 k P10 = 10-turn potentiometer, 50 k or 100 k

Capacitors: C1,C2 = 3n3 C3,C4,C5 = 100 n Semiconductors: D1,D2 = DUS

T1 ... T10 = BC 556, BC 557 IC1 = 74LS192 IC2 = 74141

IC3 = 7447 IC4 = N1 . N4 = CD 4093 Display = HP 5082 · 7750 (common anode) goes low.

Construction

number on the counter outputs by 1.

The outputs of the counter are connected

to a BCD-decimal decoder/driver (IC2).

Depending upon the BCD input data.

one of the outputs of this IC will go low.

The counter outputs are also connected

to a BCD-7-segment decoder/driver,

which in turn is connected to a

7-segment display. In this way the state

of the counter (and the output of IC2

When one of the outputs of IC2 goes

low, the corresponding transistor is

turned on. The emitter voltage of the

transistor is determined by the position

of the associated potentiometer wiper.

Only a small saturation voltage is dropped across the transistor. The

output voltage of the circuit (i.e. the

tuning voltage for the vericen diodes)

can thus be set by edjusting each poten-

tiometer to give the appropriate voltage

when the corresponding output of IC2

Altogather 9 preset potantiometers are

used, which means 9 preset stations, If

no prasat station is required (the counter

output is zero) tuning through the FM

band is accomplished by means of a

Construction of the touch tuning circuit

requires a bit of handiwork with a fret-

saw. The printed circuit board, which is

obtainable via the EPS service, consists

of three sections, which before the

components are soldared in place, must

first be sapareted from one another. On

one section of the board are four copper

convantional (ten-turn) potentiometer,

which is active) is clearly indicated.

planes, which form the two pairs of touch contacts. A second section of the

board is intended to accomodate the 7-segment display. A section is sawn out of the main board at the point where the display is to be mounted. The display board and the touch contacts are mounted perpendicularly to the edge of the mein board, as shown in the accompanying photograph. Of course the individual is free to choose an alternative design for the touch switches if desired. The potantiometers used are 20-turn

presets from Piher. The existing tuning

potentiometer in the receiver can be

used for the 10-turn potentiomater.

In conclusion

Since transistors are used as voltage switches, the circuit is slightly temparatura dapendent. However most tuners have fairly good automatic frequency control (AFC), which should

input tuning voltage should not exceed 30 V. When power is applied, the circuit autometically selects channel 0, i.e. the receiver can be tuned by hand, If one wishes a praset station to be selected immediately after switch-on, than tha inputs of IC1 can be progremmed to selact another channel. For example, if pin 15 of the IC is connected to plus supply, channel 1 will autometically be

that if the display is not required, then R5 . . . R11, IC3, and the display itself

W. Jitschin

With many electronic games, such as haads-or-tails, roulette, or any of tha versions of electronic dice, a considerabla saving in battery life can be obtained by ensuring that the circuit, or at least the current-guzzling displays, are switched off efter each throw or turn. Naturally enough, it would be somewhat tiresome to have to do this by hand, so the following circuit is intended to take care of this chore automaticelly.



Basically the circuit is a simple timer. Pushbutton switch S1 is the start button for the die, roulette wheel, etc. Whan depressed, it causes capacitor C1 to charge up rapidly via D1. Transistor T1 is turned on, so that, via T2, the ralay is pulled in, thereby providing the circuit of the game with supply voltage.

Whan the switch is released, initially nothing will happen. C1 discharges via R1, R2 and the base-emitter of T1, however it takes several secondes until It has discharged sufficiently to turn of T1. Whan it does so, however, the relay drops out, cutting out the power supply to the die, etc.

With the component values shown in the circuit diagram, a delay of roughly 3 seconds is provided in which to read off the display. If that interval is too short (or too long), it can be modified es desired by choosing different values for C1 and/or R1/R2.

ensure that this is not a problem The supply voltage is 5 V, whilst tha

selected.

Finally, it is perhaps worth remerking can of course be omitted.

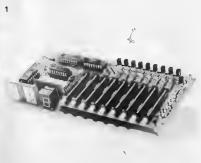


Photo 1. A section of p.c.b. is sawn out of the main board at the point where the display board, accommodeting the 7-segment display, is to be mounted.

10-10 — elektor october 1979 umpedance bridg



It is often very useful to be ebla to match tha values of capacitors and resistors and the only quick, effective way to do this is by using an impedance bridga. The following circuit is quite adequate for this purpose and it is also capable of measuring resistances between 100 Ω and 1 M and capacitances between 100 Γ and 1 Γ and

Measuring resistanca

Most readers will be familiar with the basic Wheatstone bridge circuit shown in figure 1, which represents the simplest way of measuring an unknown resistance. The bridge is formed by two pairs of resistors (voltage dividers) which are connected in parallel. As every reader will know (we hope), when two resistors are connected in series, the voltage dropped across each resistor is proportional to the value of that resistor. Thus if the resistors are connected as shown in figure 1 and we ensure that the ratio of Ra and Rb to Ry and Rc is the same, the voltages at points A and B must also be the same. To put it enother way, for the bridge to be 'balanced' and the meter to read zero voltage between points A and B, Rax Rc must be the same as Rx x Rb. If now we make Rb variable and provide it with a calibrated scale, then by adjusting Rh until the meter shows zero deflection we can determine the value of the unknown resistance, Rx.

Measuring capacitance

Measuring capacitance is slightly more complicated than measuring resistence, however the basic principle involved is the same. A capacitor also possesses resistance to current flow, which is called its reactance, and like resistance is measured in Ω. Unlike a resistor, however, it is only meaningful to talk of a capacitor's reactance to alternating current, since capacitors do not pass steady current at ell. Furthermore, the reactance of a given capacitor is frequency-dependent, i.e. the greater the frequency of the voltage across it, the lower its reactance, and vice-versa. For this reason, we have to ensure that the supply voltage to our Wheetstone bridge is alterneting end of constant frequency (it of course makes no difference to a resistor whether the voltage is AC or DC). Once that is the case, the reactance of the capacitor is determined solely by its capacitance. Thus if we replace the unknown resistance, Rx, by the unknown capacitance, Cx, and one of the fixed resistors in the bridge by a fixed capacitor, we can determine the value of Cx from the setting of the calibrated variable resistor, Rb.

Since the capacitors are connacted in series with a resistor, strictly speeking the meter is measuring *Impedance*, hence the name, impedance bridge. When the variable resistor is adjusted for zero deflaction on the meter, Wheatstone's formula once again applies, i.e.: $Z_X : R_B = R_B : Z_C$, where Z is the symbol for impedance (in S).

Circuit

The complete circuit diagram of the impedance bridge is shown in figure 2. As already explained, a resistance remains the same, regardless of whether the voltage source is steady or alternating. Thus we can choose an alternating supply voltage for the bridge. In order

to be eble to measure fairly smell capacitance values, a reasonably high frequency (significantly higher than the mains frequency) is required, and to this end e Wien bridge oscilletor, formed by the circuit round op-emp A1, is used. When the gain of the op-amp is x 3, the oscillator produces an elternating voltage with a frequency of roughly 1 kHz. The gain of the op-emp cen be veried by meens of P1, thus ensuring that the oscillator can always be started. Ideally P1 should be adjusted such that the circuit just oscillates end no more. If desired the oscillator output can be examined on an oscilloscope and P1 adjusted for as sinusoidal a weveform es possible, although this step is not strictly necessary. A2 functions as a buffer stage, delivering sufficient power to drive the bridge.

The Wheattone bridge is clearly recognisable in the circuit diagram. If we compare it with the circuit of figure 1, it is apparent their resistor R_i is registed by four different value resistors, each of which can be selected by the arrage of which can be selected by the arrage that the circuit of the comparent of the compare

The fixed value capacitor in the bridge is formed by C8. This capacitor is connected in series with another potentiometer, P3. During the measurement procedure, when P2 is being adjusted for zero deflection on the meter, P3 is set for zero resistance. Once the measurement has been completed, the quality of the unknown capacitor (Cx) can be determined with the aid of P3. How this is done is discussed in the section on using the impedance bridge. The voltage between points A and B in the circuit is measured by the differential amplifier A3. C6/R17 and C7/R15 ensure that only the 1 kHz alternating voltage appears across the inputs of A3. The output of A3 is fed via C9 to A4, which in conjunction with D5 provides a half-wave rectified voltage, suitable for driving the meter (which in fact displays the average value of the rectified signal).

Construction

It should not be difficult to construct the circuit using Vero-board or similar. If the circuit is mounted in the same box as the power supply, then care should be teken to plece diodes D3 end D4, which stabilise the amplitude of the oscillator signal, at a reasonable distance from components which are liable to run werm. This point should not prove a serious problem, however, since the circuit only consumes some 20 mA.

Any readily available meter will prove suitable since it is not required to provide a reading which is accurate in ebsolute terms, rather it is a question of determining which setting of P2 gives the smallest deflection. The meter is being used to give e 'dip-reading'.

Using the impedance bridge

The general operation of the impedance bridge should be fairly clear from the foregoing decription of the circuit. First of ell however, the circuit must be calibrated. This is done by ediusting P1 until the oscilletor sterts. The oscilletor cen be checked by setting P4 to roughly the mid-position and connecting e wire link between the test terminals (Zx), When the oscillator sterts the bridge will cease to be in a state of



Figure 1. The besic Wheatstone bridge. In order to measure capacitance, R_G is replaced by a capacitor and the unknown capacitance inserted in place of Ry.

equilibrium (which is enother way of saving that a potential difference exists between points A and B in the circuit). It mey occur that the oscillator will stop after e short period; this simply means that P1 was not set to the optimal position and should be readjusted.

With P2 set for minimum resistance and S1 in position 4. P4 is then ediusted until maximum deflection is obtained on the meter. Diodes D6 and D7 are included to limit the current through the meter to an acceptable value; however if full-scele deflection cannot be obteined on the meter, en edditional diode can be connected in series with D6/D7. Alternatively, should it prove impossible to limit the current through the meter sufficiently by meens of P4, then D6 cen be replaced by a wire link, Once the bridge hes been set up, the next question is, how do we provide P2 with an accurately calibrated scale?

The simplest solution would be to print a suitable scale in this erticle. Unfortunately this is not really feasible, since P2 must be a linear potentiometer, and different types have a different effective electrical rotation. Furthermore the first and last sections of the potentiometer tracks are not completely lineer, end the extent of the nonlinearity varies from potentiometer to potentiometer. For these reasons it is better to experimentally determine a suiteble scale oneself.

First of all, \$2 is set to position R (measurement of resistance). S1 is then set to position 1 end e series of close tolerence resistors with velues renging from 100Ω to $1 k\Omega$ are mounted between the test terminels. For eech resistor, P2 is adjusted until the bridge is belenced (i.e. minimum deflection on the meter). At the corresponding position of P2 a merk is drewn on the scale, eccompanied by the first two figures of the resistor value seperated by a full-stop. For example, if Rx equals 470 Ω, one writes 4.7. For the different positions of the renge switch, S1, the following multipliers give the correct magnitude of the velues:

position 1 x 100 Ω position 2 x 1 kΩ position 3 x 10 kΩ

position 4 x 100 kΩ The celibration procedure need only be

carried out for one range; thereefter the scale will also be correct for the other ranges To calibrate the scale for capacitors, \$2 is set to position 2 and P3 adjusted for

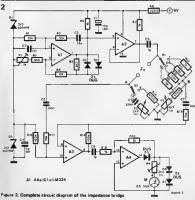
zero resistance. Close tolerance capacitors between 1 n end 10 n are then connected between the test terminals in turn, and P2 adjusted for minimum deflection on the meter. Once egein the scale is marked at the corresponding positions of P2. For the value 1 n. switch S1 should be set to position 4; for larger values up to and including 10 n, position 3 is required. The scele will 'run' in the opposite direction to that for resistors, i.e. the scale will decreese from 10 down to 1 from left to right, wherees with resistors it increases from 1 to 10.

The multipliers for each position of the

range switch are: position 1 x 100 n position 2 10 n ×

position 3 1 n × position 4 x 0.1 n

Capacitance is not the only quantity which can be measured, however. Once the value of the capacitor has been established, it is possible to obtain an idea as to the quality of the capacitor. This is done by adjusting P3 (which during the meesurement of capecitence is of course set for zero resistance). If by so doing the deflection on the meter can be made even smaller, then the further the deflection can be reduced, the poorer the quality of the capacitor.



As usual, each program is preceeded by a succession of 1200 Hz tones, to indicate the program number.

Program 1: Luna (R. Bayer)

This progrem simulates the landing of the LEM (Lunar Module) on the moon, The display gives information on the height above tha surface, the rate of descent end the amount of fuel left in the tank.

The maximum thrust available from the engine is limited, so that leaving raverse thrust too late will result in a crash landing. The maximum permissible descent rete at the moment of touchdown is 01: if this is achieved, the display will alternate the final results with the message 'lended'.

It is not an easy metter to control a LEM, and the result is that landings may well be rougher than intended. In thet case, the message on the displey will

new programs for the SC/MP



Good news for SC/MP fans: two new records have been edded to the ESS range. One contains the complete NIBL E program; the other includes some gemes, a 'running script' progrem, 'tracer', 'disassembler' end 'biorhythm'. Some further details on the latter programs are given here.

The keyboard is used to control the reta of descent. When the program is started (at eddress @C@@), the text 'Luna' eppears on the display. The game is then started by operating any one of the kays on the HEX I/O keyboard; the display now gives all relevent information. The first three digits (reading from tha left) indicate the height of the LEM. The fourth digit is always off; the fifth and sixth give the present rate of descent. Finally, the seventh digit is off end the eighth gives the remaining fuel.

The power output of the engine can be controlled with keys 0 . . . 7. It is the intention to use the engine to braka down to a soft landing, but it should be noted that over-enthusiastic 'reverse thrust' can reverse tha direction, so that the module sterts to move away from the moon! A further point to watch is that operating tha '0' key shuts off the engine... aftar which it cannot be restarted! The initial thrust of the engine is set by the program to '2', with the result that the LEM picks up speed towards the surface quita rapidly.

leave no doubt: 'creshed'!

There is another way thet things can go wrong. If too much thrust is used too soon, the fual supply may run out before touchdown. This is indicated by an 'F' in the last digit (for 'fool'?), after which the speed will gradually pick up to the fatal moment of impact . . . 'crashed'!

If the loudspeaker interface is included in the SC/MP system, the progrem will provide some suitable sound effects. The thrust that the motor is putting out can be recognised from the frequency of the rattle coming out of the loudspeaker. A cresh landing is accompanied by a lot of noise, that can be interpreted as an explosion. The higher the speed at the moment of impact, the longer the racket will last

Would be astroneuts have an option not available to their real-life counterparts. If it becomes obvious that things are getting out of hand, the lending can be interrupted by operating one of the other keys (other than 0 . . . 7). The original 'Luna' display then re-eppears, after which a new attempt can be initiated by operating any one of the keys.

Program 2: Battleships (F. Schuldt)

'Battleships' is normally a game for two players. In this program, the computer takes the role of one of the players.

The game is played on a 64-squere 'ocean', as shown in figure 1. In all, six ships take part in the engagement: two of three squares each, two of two squares and two of one square each, The ships may only be entered in horizontal or vertical direction, and they are not allowed to touch.

When the program is started (at address 0C40), the word 'Ships' appears in the display. As soon as env key is operated, the computer draws in its own set of ships in its mamory. It then invites Its opponent to take the initiative: 'Fire'. The coordinates of the first square to come under fire can now be entered:

first the line number and then

the column number (or

letter). The computer can

1. If the shot landed on one of its ships,

it will display 'Hit'. After a brief

delay, it will invite a further try:

line and column numbers, respectively. The player can now answer in

three ways 1, A hit is recognised by operating the 'Down' key. The computer will reply

immediately with 'shot XY' 2. Operating the 'Up' key indicates that a ship is sunk. This, too, will be

ecknowledged with another shot. 3. A miss is indicated by operating any

other key. The computer will tell you to get on with it, in that case: 'Fire'. As soon as all ships of one of the sides

are sunk, the word 'end' will appear on the display. After a brief delay, the program will reset and the word 'Ships' will appear.

Program 3: Keyplay (F, de Bruijn) This game is known under a variety of names, 'NIM' being one of the most popular. It can be played with matchsticks, coins, or . . . numbers. The rules are simple: each player in turn subtracts a number from the original; the one to gat 0 as result, wins.

When the program is started, at eddress ØCØØ, the program will ask for a four-digit decimal number ('GE' = Give Entry): this is the number from which the players will subtract in turn. Next, the program will want to know the Limit

('LI'): this is the maximum number that may be subtracted at one time.

The human player is ellowed to start. This is indicated by 'U' in the first display digit. A four-digit number can now be entered. If it is either 0 or mora than the limit, the computer will refuse to accept it: it will display the word 'reject', followed by a repeated request 'U'. If a valid number is entered, the computer will perform the subtraction and display the result: 'SAxxxx', where xxxx is the remainder, It then calculates the number that it wants to subtract, and displays this with the prefix 'I'; finally, it performs this subtraction end again displays the result as 'SAxxxx'. It is now the human player's turn, end the game continues until the remainder becomes equal to 0. Depending on who reached this point, the display will indicate either 'I LOSE' or 'U LOSE'.

The program can be re-started by operating the Halt/Raset key.



This program can display up to 16 different lines of text, each consisting of up to 256 characters, as a 'running script' on the 7-segment displays.

The start address for the program is @C@@. Initially, 'runtaxt' appears on the display. One of the keys O . . . F is now used to select the desired one out of the sixteen texts. Even when a text is running, it is possible to switch over immediately to any other text, by operating the corresponding key.

The program consists of three parts:

- 1. A selection routine, that uses the Elbua LDKB1 routine to determine which of the texts is required. It places the start address of the text in pointer 2, and the length of the text in a memory location reserved for this purpose (es can be seen from the listing).
- 2. A display routine, that transfers the text (pointer 2) to the display (pointer 1). This routine also checks to see if a different text is required (key entry); as long as this is not the case, the text originally selected is repeated. The speed at which the text runs across the displays can be varied within wide limits by modifying the contents of addresses @D48 and @D57. 3. The text section, containing the texts
- in 7-segment format. Each charecter is stored in one memory location (8 bits). The texts all start with seven spaces (00), so that e new text always starts on a blank display.

When this program is loeded from the ESS record, not only sections 1 and 2 (as given in the listing) are entered, but elso several texts. For this reason, the memory is used up to and including location @E33.

Program 5: Biorhythm (H. Prante) A few years ago (in October 1977), Elektor published a program for calculating biorhythms on an HP65 calculator. Now, a similar program is evailable for the SC/MP system.

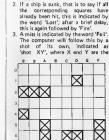
As usual, the program is started at eddress @C@@. Initially, the word 'today' appears; the date for which the biorhythm deta are required should now be entered. The date should be entered in the following order: day, month, year (without '19'). This entry is immediately followed by the display 'birthday'; this date is entered in the same way.

The computer performs the necessary calculations and displays the results: three numbers, corresponding to the physical, amotional and intellectual rhythms. A new calculation can be performed after operating the Halt/Reset kav

The biorhythm theory was explained in the earlier article referred to above, but a brief reminder may be in order. The physical rhythm has a cycle of 23 days; the emotional cycle is 28 days the intellectual cycla lasts for 33 days. The 'zero crossings' are critical days, and these include the half-way marks: 11th . 12th day for the physical cycle, 14th for the emotionel and 16th . 17th for the intellectual. The first half of each cycle is taken to have a positive influence; the second half is negetive.

Program 6: Tracer (J. Fischer)

This program is a powerful extension of



reply in three ways:

'Fire'

the monitor software already available in the SC/MP system. The CPU routine in Elbug can only handle one breekpoint. and it must be reset every time it is used.

'Tracer' constitutes e much more powerful eid when de bugging programs. It can be used to execute any other progrem in 'single-step' mode. The program under test is thus executed instruction-by-instruction; between instructions, the contents of all registers cen be examined (P1, P2, P3, Accu, Extension Register, Status Register). The display gives information on the position of the progrem counter and the following instruction, before actually executing it. If errors are noticed at this point, it is possible to correct them before continuing the single-step scen.

The single-step mode can be executed in three weys:

- 1. High Speed: The program to be tested is executed at a rate of approximately one instruction per millisecond, until e specified address is reached. At this point. 'Tracer' autometically switches over to the 'Low Speed' mode. The display is blanked during the High Speed mode
- 2, Low Speed: The address and the corresponding instruction are displeyed for approximately one second. The instruction is then executed, and the display is blanked for one second. This sequence is repeated until the point is reached where the change-over to 'Manuel Step' is required. This will occur eutomatically at a specified eddress; however, it is possible to effect en earlier switch to the Manuel Step mode by operating any of the keys during the Low Speed mode.
- 3. Manual Step: The next address and corresponding instruction remain visible in the display until one of the keys (env key except the CPU-routine key) is operated. The address and instruction remain visible for about one second after the key is operated: the instruction is then executed and. after a brief delay, the next address end instruction appear on the display.

in all three modes, the keyboard and display remain available for in or output of data.

When 'Tracer' is sterted (at address OCOO), the message 'SS . . . ' appears on the display. Three addresses should now be entered, in the following order:

- 1. The 'start addrass' of the program to be tested:
- 2. The address et which the change-over to Low Speed is required;
- 3. The address et which the Manual Step mode must be initiated.

After the third address has been entered, operating env one of the keys starts the Tracer routine. The first section of the program will be run through in the High Speed mode, unless the second eddress is equal to the start address (1). In the High Speed mode, the keyboard and display seem to function normally. In the Low Speed and Menual Step modes, this becomes rather more

complicated. In the Low Speed mode, the keyboard must be operated in the time that the instruction (and eddress) are visible on the display. In the Manual Step mode, the keyboard becomes operational when the command is given to execute the instruction: it remeins eveilable for approximately one second, until the display is blanked and the instruction is executed,

The time during which the display is blanked by Trecer (for one second efter the instruction is executed) is used to show the displey that the progrem under test would provide efter that instruction is executed. However, it should be noted that the display is egain used by Trecer before coming to the next instruction, so that all previous displey date is lost and the 'program display' can therefore consist only of single digits.

Both the Low Speed and Manual Step modes can be interrupted to check the contents of ell registers in the CPU. In the Low Speed mode, it is first necessary to switch over to Manual Step, by operating one of the keys. The display will then show the eddress end instruction that is about to be cerried out. If the CPU-routine key is now operated, the displey 'CP' will epppear. The keyboard can be used at this point to select one of the registers; the codes are the same as those used in the Elbug CPU routine: '1' = Pointer 1, '2' = Pointer 2, '3' = Pointer 3, '5' = Status Register, 'A' = Accu, 'E' = Extension Register.

There are various ways to leave the CPU routine:

S(ubtrect)-key: Tracer can be re-started. R(un)-key: Return to High speed, Tracer now expects the entry of two addresses: one to indicate the point et which it must switch over to Low Speed and one which specifies the first address of the Menual Step mode.

Heying re-started Tracer in aither of these ways, all the facilities described above are available again.

Program 7: Disassembler

(F. de Bruiin)

A disassembler is a program that can be used to obtain listings (without comments, obviously) of programs in machine language. It is the opposite of an assembler program.

The listing can be obtained on a printer or an (Elek-)terminal. In the latter case. of course, no 'hard copy' of the print-out will be obtained.

The serial output signal for the printer or video display is available at flag 0. The transmission rate is 300 beud. This speed can be modified, if required,

accordin	g to the	following	table:	
	110	300	600	1200
eddress	baud	baud	baud	baud
159 B	97	64	25	86
159 D	17	06	03	01
15A7	89	FØ	50	81
15A9	08	02	01	00

The (11/2 K) program offers the following facilities:

- a) enter the 'begin address' of the progrem that is to be 'disassembled'; b) specify the begin and end addresses
 - of e table; c) mark a byte used by the program, by
 - entering '20' at that point; d) enter the number of consecutive lines

to be disassambled. The program is started at address 1000. When 'D1 , , , ' eppears on the displey,

the begin eddress can be entered. This can be followed, if necessary, by specifying one table; in that case, tha Block Transfer key must first be operated - if eny other key is operated, the program essumes that there is no table. After the Block Transfer key, the begin address of the table is entered, followed by the end eddress plus one.

The next step is to specify the number of lines to be printed: note that this number must be entered in hexadecimal. A suitable value, when using the Elekterminal for the display, is \$610. The maximum value is GOFF; this already mekes for quite e lengthy print out.

The program will start the print-out immediately after receiving this final entry; it will stop when the specified number of lines have been disassembled. A further group of lines will be disassembled if the Halt/Reset key is operated,

If the program finds en instruction that it doesn't recognisa, it will print '7', Jump instructions by meens of the program counter ere shown with the address to which the jump would be executed. The same applies to other instructions that use the program counter.



digital rev counter

A. Ohde

In most cars tha angina speed (r.p.m.) is displayed on an analogua scale. However, a digital readout, using sevan segment displays, is also perfectly possible.

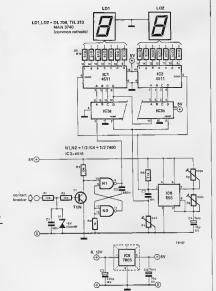
Teble 1

8 cil 4-stroke

Engine type	Input frequency for 6000 r.p.m.	10V5 0 50 Hz
1 cil2 stroke	100	3000
2 cil. 2-stroke	200	1500
3 cil 2-stroke	300	1000
1 cil. 4-stroke	50	6000
2 cil. 4-stroke	100	3000
4 crl. 4-stroke	200	1500
6 cil. 4-stroke	300	1000

750

The circuit shown here provides a two digit display calibrated in hundredsof-revs per minute, i.e. 6000 r.p.m. will produce a readout of 60. There are two principal reasons for restricting the display to two digits. The first is quite simply that accuracy greater than this is not necessary, and secondly, a much longer gate time would be required otherwise, with the result that the counter would not be able to follow sudden changes in the engine speed. The circuit is a modernised version of a rev counter published in an earlier issue of Elektor (see Elektor 1. December 1974). The input signal is derived from the contact breaker; the amplitude of the resulting pulse train being limited by zener diode D1 and then 'shaped' by T1 and the monostable



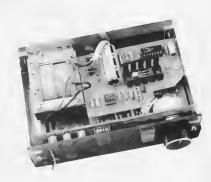
N1/N/2. The pulses are counted by IC3 (dual decade counterly, whose outputs are connected to two BCD-to-Psegment latches/decode-drivers. The reset pulse for the counters lie, the timebase provided by a \$55 timer (IC5).

The circuit has three adjustment points. Preset potentiometer P1 sets the width of the reset potentiometer P1 sets the width of the reset pulse. In the majority of

of the reset pulse. In the majority of cases it will be sufficient to set this potentiometer to the mid-position. However it may happen that the reliability of the circuit can be improved by choosing an attenative position. The latch period, and hence the rate at which successive measurements are displayed, is set by means of P2. Finally, P3 is used to calibrate the counter. This can be done using either a tone generator with a calibrated tuning scale, or else by using a mains frequency signal, In the former case the frequency of the input signal will depend upon the type of engine with which the rev counter is to be used. The counter is calibrated for e nominal r.p.m. of 6000, and cepending upon the number of contact breaker pulses produced for each revolution of the engine in question, a signal of suitable frequency (see table 1) is fed to the input of the circuit and P3 adjusted until a readout of 60 is obtained. If a tone generator is not available, a low voltage signal of mains frequency (e.g. from a doorbell transformer) can be used. P3 is then adjusted until the appropriate readout is obtained (see table 1, 'revs at 50 Hz').

digifarad

digital capacitance meter



Given the fact that many types of capacitor — especially electrolytics have a wide tolerance (20% is fairly common), it is often desirable to be able to measure capacitances both quickly and with a reasonable degree of accuracy (e.g. when constructing precision timer circuits, matching the time constants of several RC networks, etc). Of course a capacitance meter also enables one to measure the value of those piles of unmarked capacitors which end up at the bottom of one's junk box, or to test 'suspect' capacitors for potential faults — in short it represents a useful addition to the test ear of any constructor.

The circuit described here offers the advantages of a digital display, has 5 decade ranges, measuring from 1 nF to 9.999 μ F, and is accurate to about 2%.

The range of digital test equipment is growing ever more extensive. Voltage, current, frequency, resistance, temperature — all thase quantities are now commonly measured, and displayed, digitally. This not only applies to 'professional' applications, even the 'maneture constructor' has gone digital (see, for example, the 'universal digital metar', Elaktor 45). Now it is time to add a digital expectance meter to the

range - the 'digifarad', The block diagram of the 'digifared' is shown in figure 1, Cx represents the unknown capacitance to be measured. Depressing the 'start' button momentarily closes the electronic switch, ES, so that Cx is charged to a given voltage (Uc). When ES reopens, Cx is discharged by a constant current source (I), with the result that the voltage on Cx falls in e linear fashion. All other things being equal, this discharge rate is datermined by the value of Cx. The voltage on the cepacitor is monitored by a window comparetor, formed by two op-amps and a set/reset flip-flop. For the period that Uc ramains within the upper and lower reference voltages (U1 and U2) of the 'window', the output of the comparetor is low. This enables a three digit counter, which counts the number of pulses from e clock generator. Thus the graeter the capacitance of Cx, the longer Uc takes to fall below the threshold voltage of the window comparator. end the more pulsas counted by the counter. Finelly, by varying the size of the constent current, I, we can arrange for capacitors of widaly differing value to be meesured in the same wey.

Tha complete circuit diagram of the digitard is shown in figure 2, and a pulse diagram is given in figure 3. The latter is not only useful in the (unlikary) event that trouble-shooting proves encessary; it is also great help in the following axplanation of the circuit. The verious wave-hapes (A. ...!) were measured at the corresponding points in the circuit.

It is not too difficult to relate the block diagram, given in figure 1, to the actual circuit shown in figure 2. The constant current source, 1, is formed by op-amp A1 end transistor T1. The size of the current is determined by the position of the range switch, S1 (see table 1). The op-amp varies the current through T1 more position of the range switch, S1 (see table 1). The importance of the range switch, S1 (see table 1). The importance of the range switch, S1 (see table 1). The importance of the range switch and the range of the

The electronic switch, ES, consists of transistor T2, which is turned on via the start button, S2, and flip-flop N3/N4. The voltage on C2, is buffered by op amp A2, and fed to the window compartor formed by A3 and A4, N1, N2, C1, C2, R18 and R19 form a set/reset lift pflop which is triggered by changes of the N1 of N

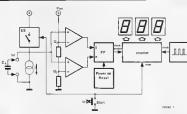


Figure 1. Block diagram of the digital capacitance meter. The unknown capacitor, C_{χ_i} is discharged by a constant current, 1. The longer the discharge period the more pulses counted.

However when the voltage on C_x rasche the upper threshold of the 'window' (i.e. the voltage on the non-inverting injurt of A2 falls below that on the inverting injurt) of A2 gas to the inverting injurt) the output of A2 gas town with the result that the output of N2 also goes low, enabling the counter. To discharge, the voltage on C_x voltage on

In eddition to turning on T2, the second flip-flop formed by N3 and N4 provides

the counter. The displey is inhibited during the count cycle, thus ensuring e stable readout. R2D, C3 and the two diodes (D1 and D2) ensure that the two flip-flops essume the correct state upon switch-on.

The clock-signal for the counter is provided by a 555 timer (IC3) connected as an asteble multivibrator. The counter itself (IC6) is a single IC, type 74C925. It performs the 7-segment decoding, end drives the three LED displays wis transistors T4... T6. The displays ere of the common cathode type (e.g. HF 5082-7760, DL 704, etc.).

for the circuit: the reference voltage $(U_{\rm ref})$ end the 16 V, 12 V end 5 V supplies. The obvious solution is to use IC's: one three-pin regulator (IC5) takes cere of the 12 V supply, and e 'basic' 723 circuit (IC4, T3) provides ell the other voltages, including the reference voltage.

Construction

Once again, printed circuit boards (eveileble through the EPS service) reduce constructional problems to a minimum, Every single component, barring the meins transformer, is mounted on these boards - from supply circuit to displays. To increase the sense of echievement, three boards ere required instead of one. A display board (figure 4c) is mounted behind the front panel, and the other two boards (figures 4a and 4b) ere bolted together with spacers in a sandwich construction and mounted behind the display board. The display board contains the displays, Obviously. It also provides space for IC6, resistors R31 . . . R37, switches S1, S2 and S3; furthermore the on/off indicator D8 and 'banana plug' connection sockets for the unknown capacitor Cx. The upper board in the sandwich (figure 4b) is intended for the supply circuit (all except IC5) and the clock generator, IC3, Finally, the lower 'sandwich' board (figure 4e) must provide space for the remeinder of the circuit. Rest essured: it does. The interconnections between the verious boards

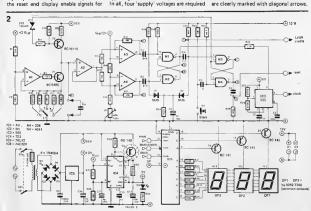


Figure 2, Complete circuit diagram, Common cathode type displays are used.

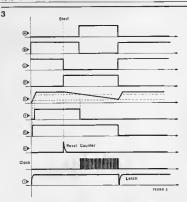
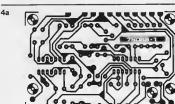
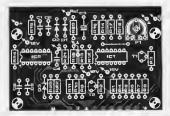


Figure 3. In this pulse diagram, the letters A . . , I refer to the corresponding test points indicated in figure 2.





Parts list

Resistors R1 = 56 k

B2 = 68 k R3,R11,R21,R23,R28 - 4k7

R4 = 390 A R5 = 3k9

R6 = 39 k R7 = 390 k RB = 3M9

R9 = 100 Ω B10.B15.B24 = 4k7

R12,R13,R14 = 10 k R16,R17,R22 a 1 M B18 B19 B20 = 100 k

R25,R26 = 470 k R27 = 2k2

B29 = 56 Ω R30 = 0.56 Ω R31 . . . R37 = 10 Ω (see text)

R38 = 22 k

R39 = 270

P1 = 47 k preset potentiometer Capacitors:

C1,C2,C4 = 2n2 C3,C11 = 1 µ/16 V C5,C6,C7,C13 = 1 n

C8 = 100 n C9 = 1000 µ/25 V

C10 = 10 µ/16 V C12 = 10 µ/6 V

Semiconductors

IC1 = 324 IC2 = 4011

IC3 = 555

IC4 = 723 (DIL)

IC5 = 78L12 ICB = 74C92B

T1 = BC 109C, BC 549C, or equ. T2 = BC 161-18

T3 = BD 140 (with heetsink!) T4,T5,T6 - BC 141

D1.D2 = DUS D3 = BV3/400 mW zener diode

D4 . . . D7 = 1N4004

DB = LED DP1 ... DP3 = common-cethode

7-segment displays. 9 a HP 5082-7760

Sundries:

S1 = 5-way, single pole selector switch

S2 = pushbutton switch, single pole

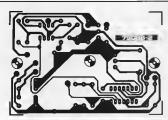
\$3 = two-pole mains switch Tr = 12 V/1 A meins transformer (see text)

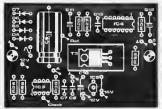
500 mA slo-blo fuse

Toble 1

measurement scele position current I range multiplication fector 1 μΑ 999 nF 1 nF 2

10 µA 9 99 µF 0.01 µF 3 100 µA 99.9 µA 0.1 µF 1 mA 999 µA 1 µF 5 10 mA 9 99 mF 10 µF





Final notes

The capacitance metar is as easy to use es a multimeter; switch it on with S3, select the desired range with S1, connect the unknown capacitor, press the stert button (S2) and watch the result appear on the display. The measuring ranges are listed in the Table; the current I listed in this teble is the constant-current used to discharge Cx. If the capacitance value is completely unknown, it is a good idea to start in tha highest range (position 5), and then switch back step-by-step until a useful reading is obtained.

The circuit contains only one calibration point, namaly preset potentiometer P1, Calibration can be carried out with the aid of a close tolerance capacitor of a known value. Silvered mice capacitors, for example, typically have a tolerance of 1%.

One final remark, If a 12 V/1 A transformer is felt to be rather heavy, or if a smaller transformar happens to be available, resistors R31 . . . R37 can be modified as required, Provided e slightly less brilliant displey is considered adequate, the value of these resistors can be increesed to 22 Ω; a 12 V/½ A transformer is then good enough.

4c

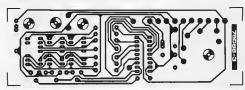




Figure 4. The three printed circuit boards required. The main board (figure 4a) and the supply end clock generator board (figure 4b) are mounted in a sandwich construction, using spacers. They are then coupled to the display board (figure 4c) that is mounted behind the front penel.

short-interval light switch

Even in today's well-equipped modern houses there are various 'corners' where additional lighting is required. For derk cupboards, meter boxes etc. temporary lighting is usually sufficient, so that making a connection to the mains is hardly worthwhila; a simpler and cheaper solution is to use a battery-powered circuit which will light a lamp for a short period of time. As is apparent from the accompanying circuit diagrem, such a circuit is by no means complicated, Using only one CMOS IC, three resistors and one capacitor, the circuit will switch on a lamp for a presettable interval

The operation of the circuit is perfectly straghtforward: when the button is pushed C1 charges up to the supply voltage. The outputs of the four parallel-connected inverters (N3 . . N6) are then low, so that the lamp will be lit. When the button is released, C1 discharges via R1 until the input of N1 reaches half supply. The Schmitt trigger formed by N1 beautiful that the lamp is extroguished. The positive feedback resistor R3 ensures that the Schmitt trigger changes state very quickly. With the resistor values shown in the

circuit diagram, the lamp will remain lit for roughly 2.5 saconds per μ F of C1.

1

Thus a 10 μ capacitor would give an interval of roughly 25 seconds.

The circuit can be powered by four 1.5 V cells connected in series. If a larger lamp is required, three 4.5 V cells connected in series can be employed. Altarnatively, for really 'heavy-duty' applications, the four parallel-connected inverters can be replaced by a trensistor, as shown in figure 2. The supply voltage should be matched to the voltage rating of the lamp end may lie between 4.5 and 15 V. The current through the lamb should not exceed 500 mA in that case.

A 5 BC 141

PCB. for variable fuzz box

The design for the 'variable fuzz' box' was first published in the December 1978 issue of Elektor. Such is the popularity of this circuit, that we have decided to produce a printed circuit board for it.

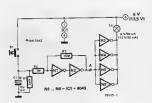
The variable fuzz box is a special effects unit for guitarists, which by allowing the emplifier signal to be clipped in everlaty of different ways (symmetrically, asymmetrically, soft, hard, etc.) offers e greater degree of control over the resultant sound. The circuit of the fuzz box was described in detail in the original article, hence will not be repeated here. However one correction to the original description has to be edded: symmetrical clipping of the output signal produces only uneven (not even, as was stated) harmonics, whilst asymmetrical clipping generates both even and uneven harmonics in the output signal.

spin siturative circuit diagrams of the fuzz box for symmetrical filipure 3 of originel erticlel and symmetrical filipure 4 of originel erticlel power supplies are here combined into one (see figure 1). The circuit diagram contrains a number of lettered connection points (a...h, j. k, m...w) which are marked on the printed circuit board shown in figure 2. The circuit diagram and accompanying parts list provides the relevant details on which connections should be mede for either symmetrical or symmetrical power supply require or symmetrical power supply require

The current consumption of the circuit is less than 20 mA. A 741 can be used for IC1, however an LF 356 is a better choice.

Literature:

Variable Fuzz Box, Elektor 44, December 1978



2

1

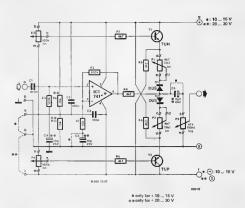


Figure 1, Circuit diagrem of the verieble fuzz box for symmetrical and exymmetrical power supply stages.

2

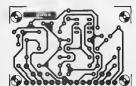




Figure 2, Printed circuit board for the variable fuzz box. The one board is suitable for both versions of the circuit.

ports list

Resistors R1.R9¹.R10¹ = 10 k

B2.B3 = 100 k R4, R5, R6, R7, R8 = 4k7

Potentiometers P1,P2 = 4k7 (5 k) lin. P3.P4 = 100 k lin. P5 = 47 k (50 k) log

Capacitors: C1 = 470 n C2.C3 = 100 n

C41 = 22 µ/25 V C51 = 10 µ/25 V C62 = 2u2/40 V

Semiconductors: IC1 = 741 or LF 356 (see text) T1 = TUN

T2 = TUP D1.D2 = DUS

Wire links

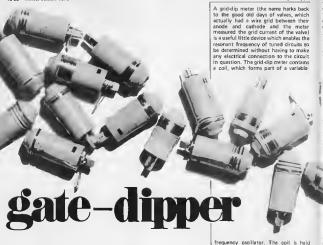
asymmetrical supply voltage + 20 . . . 30 V: points q and t symmetrical supply voltages ± 10 . . . 15 V: points q and k C5 replaced by link C6 replaced by link

Remarks:

I amitted in the case of symmetrical supply voltages.

² replaced by wire link in the case of symmetrical supply voltage.

10-22 -- slektor october 1979 gate-dipper



the modern equivalent of the grip-dip meter provides a quick way of checking the resonant frequency of LC tuned circuits near the parallal-resonant circuit (the equipment containing the tuned circuit should be switched off for the purposes of the measurement), Series-resonant circuits can also be measured by shorting their inputs, so that a parallel-resonant circuit is obtained. The coil of the griddip meter is electromagnetically coupled to the resonant circuit. As the frequency of the oscilletor approaches the resonant frequency of the LC circuit, so tha oscillator becomes increasingly damped. This is registered by the meter, so that when the needle daflection is at a maximum, and the oscillator frequency coincides with the resonant frequency of the tuned circuit, the latter can simply be read off a calibrated scale.

The circuit of the gate dipper described here is based upon a device known as a lambda diode. As many readers may well never have heard of such a 'beast' it is worth devoting a little time to an explanation of this slightly unusual circuit element.

Lambda diode

If the term lambda dlode is unfamiliar, the majority of our readers will have heard of tunnel dlodes. These are diodes which exhibit a negative resistance over a certain portion of their voltage-current characteristic. The concept of a negative resistance may seem confusing, but in fact it is quite straightforward. As the

Tuning resonant circuits in high frequency equipment normally requires fairly expensive test gear which not every hobbyist can afford. However there is a reasonably cheap alternative available, namely a gate dipper, which allows the resonant frequency of the tuned circuit to be ascertained simply and quickly.

voltage dropped across a 'normal' or 'positive' resistance increases, there is a directly proportional increase in the current flowing through that resistance. A negative resistance, however, ensures an inversely proportional relationship between voltage and current, i.e. the current increases as the voltage decreases. The typical voltage-current characteristic of a tunnel diode is shown in figure 1. Dver the range -r the diode exhibits a negative resistance. Assume for example that the diode is forward biased to point P: if the voltage is now increased by A U, the current will fall by △ I. The resistance of the diode is thus:

$$-r = \frac{\triangle U}{\triangle I}$$

The negative resistance is smallest (i.e. there is the greatest drop in current for a change in voltage) at the point where the curve is steepest.

The question now is: how can we utilise



Stricity speaking, a negative resistance can be reparted as an active circuit elament (being just the opposite of normal resistance), and it is as such that tunnel cliodes are normally used. Figure 2 shows a simple example of a tunnel cliode socillator. The average current through the tunnel cliode automatically settles at a value where the effect of the settles are the stepost point of the negative resistance portion of the voltage-current characteristic. Several advantages of tunnel cliode socillators are flow power consumption, good frequency stability.



Figura 2. Only a faw components are required to build a tunnel diode oscillator. The enhances simplicity is the great advantage of the type of oscillator circuit.



Figure 1. A peculiar feature of a tunnel dioda is that it axhibits a negative resistance over a portion of its ortige v. current characteristic. When biased to this point, the dioda effectively becomes an active circuit element.

and last but not least, their inherent simplicity.

More recently however, the advant of FETs has seen the design of oscillator circuits which offer even better performanca, with the result that tunnal diodes are rarely used for this application nowadays. Despite this fact, the simplicity of tunnel diode oscillators has led to the search for ways of improving their performance whilst continuing to use the same basic principla. This attempt has resulted in the lambda diode, which consists of an N and a P-channel FET connected as shown in figura 3. Between the anode and cathoda of the device there is the same negative resistance characteristic as in tunnel diodes. Thus the lambda diode can also be used as the active element in an oscillator circuit. This is in fact the type of oscillator employed in the grid-dip meter circuit.

Gate dipper

The complete circuit diagram of the gate diopper is shown in figure 4. By using a voltage regulator (IC1) the circuit can be powered by a 9 V battery, thereby making the meter portable and essy to use. The lambda diode is formed by FET T1 and transistor T2. Since Vehancel FETs have a rafaturely shallow transfer curve, a bipolar transistor is used in its place. Although the configuration of the seme.

The configuration is the seme.

The configuration is the seme.

fixed inductor, $L_{\rm X}$, and the variable capacitor, C3, by means of which the oscillator frequency is adjusted. The lambda diode is biased to the negative resistance region by means of P1. Diodes D1 and D2 clamp the adjustment range to suitable values.

The output of the oscillator is rectified by D3. A negative DC voltage ($L_{\rm X}$ can be considered a short circuit for AC currents) appears across this diode, which serves as the control voltage for the lambda diode (via the gate of T1).

This voltage is smoothed by C4/R2 and fed to T3, which is connected as a source follower. Potentiometer P2 is adjusted such that a zero reading is obtained on the meter. If the coil, Lx, is brought near the passive tuned circuit which is to be measured, the negative voltage across D3 will fall as the oscillator is increasingly damped. This causes the source voltage of T3 to rise, thus causing a deflection on the meter. When the deflection is at a maximum, the value of C3 is an index of the resonant frequency of the tuned circuit under test. Due to the effect of the lambda diode, the behaviour of the meter needle is the opposite to that of other types of grid-dip meter, where the oscillator frequency is adjusted for minimum daflection (hence the term din meter)

The grid-dip meter can also be used to check the operation of an oscillator. Dnce again the coil of the meter is held near the oscillator circuit, and C3 is adjusted until audible best fraquencies are obtained. These low frequency best notes are not sufficiently smoothed to prevent them appearing at the source of T3, with the result that they are fad through the output stage round 14 and through the coupture stage round 15 and 15 an

When Obsection the operation of tuned circuits in real or selever, if the grid dip meter is tuned for zero bast, then it is possible to modulate the rit. signel (in accordance with the direct conversion principle). The lambda diode oscillator then functions as easif-oscillating mixer stage. This fact allows the mater to be cellorated with a precise frequency stage.

Construction

The track pattern and component overlay of the printed circuit board for the grid-dip meter is shown in figure 5. The coil, L_X, is not mounted on the board, but rether is connected to the



Figure 3. If a P-channal and N-channal FET are connected as shown, the result is a so-called lambde drade. Like a tunnal diode, this has a negative resistance over a portion of its voltage v. current characteristic.

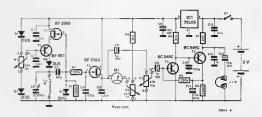


Figure 4. Complete circuit diagram of the gets dipper, FET T1 and the bipoler transistor T2 form the lambde dods. At first sight this configuration is different to that shown in Figure 3. However from the point of view of AC currents, the base of T2 is connected to the direction of T1, and the gives of T1 is connected to the collection of T2. Thus the two circuits are quivilent for the purpose of AC.

5





Figure 5. Track pattern and component leyout of the printed circuit board for the gate dipper (EPS 79514). The coil, Lx., is not mounted on the board, but rather as wound on a DIN toudspeake plug, the socket of which is mounted on the case of the meter. In this way it it a simple matter to plug in different coils to obtain different measurement ranges.

Ports ligt:

Resistors.

R1,R5 = 220 k R2 = 100 k

R2 = 100 k R3 = 3k9

R4 = 82 k

R6 = 330 Ω

R7 = 2k2

P1 = 22 k lin

P2 = 2k2 lin

P3 = 47 k log

10 4710

Copacitors:

C1,C5,C7,C13 = 22 n C2 = 47 p C3 = 220 p, varieble

C4,C10 = 100 p C6,C8 = 1 µ/10 V

C6,C8 = 1 \(\mu/10\) V C9 = 10 \(\mu/10\) V tantelum

C11 = 22 µ/6.3 V C12 = 1 n

C14 = 10 µ/16 V

Semiconductors: T1 = BF 256B

T2 = BF 451 T3 = BF 256A

T4,T5 = BC 549C

T4,T5 = BC 549C IC1 = 78L05 D1 . . . D4 = DUS

Miscellaneous:

L_x see text and table M1 = meter 225 µA (or less) S1 = on/off switch B DIN loudspeaker plugs 1 socket for loudspeaker plug circuit vie a plastic DIN loudspeaker plug. This provides the option of using several different coils to obtain different measurement ranges. The accompanying table lists the winding details for each coil and the corresponding frequency range.

The coils are wound on the plugs as far as possible from the metal terminals as possible from the metal terminals as possible from the metal terminals which increase swith frequency. The result is that after adjusting GS, the Admittelly, that is not such a distinct, admittelly, that is not such a distinct, and the meter will tend to drift. Admittelly, that is not such a distinct the meter is not being read, but merely used as an indicator to that the energy loss as an indicator to the meter will deflect to the point where no "doy" is obtained.

'dip' is obtained. The ends of the coil are fed through tha inside of the plug and soldared to the terminal pins. The coil consisting of only one turn is mounted directly on the pins, and the plastic cap is omitted, The socket for the plug is mounted on the case of the grid-dip meter end connected to the printed circuit board via short lengths of fairly thick wira. In this way it is a simple matter to interchange coils should a different measurament range be required. The variable capacitor, C3, is also mounted off board and connected to the circuit vie short, thick wiring. If the wires ere too long, maasuraments above roughly 80 MHz ere no longer possible.

Calibration and use

Before providing the gata dipper with a calibrated scale one must first know how to use it properly. P1 and P2 are set so that as positive a 'dip' as possible is obtained. The meter is here used essentially as an indicalibration of the control of

the vicinity of the coil etc.
As already mantioned, P1 in fact deter-





Figure 6. This figure shows how the coil is wound on the loudspeaker plug. The turns should be kept as far eway as possible from the metalterminal pins of the plug in order to minimise energy losses.



Figure 7. By using the grid-dip meter as an AM demodulator (working on the direct conversion principsle), it is possible to obtain an accurately calibrated trequency scale. A 10 metre length of wire is required as a suitable serial.

mines the biasing of the lambda diode, and hence the sensitivity of the circuit The optimum setting of P1 can be determined as follows:

The wiper of P1 is turned fully towards the cathode of D1. The oscillator is then inoperative and the meter defelction at a maximum. Ensure that the needle is not hard up against the end stop, however (if necessary adjust P2 accordingly). Now turn the wiper of P1 in the opposite direction. At a certain point the needle deflection will decrease (the oscillator is now running). Continue to turn P1 until the deflection is at a minimum (here again it may be necessary to adjust P2). The meter range is then set between these two extremes by adjusting P2 (nots, P2 will need to be readjusted when the coil, Lx, is changed).

To gain proficiency in using the meter it is advisable to practice with a tuned circuit whose resonant frequency is already known. At the same time one can experiment with different settings of P1 to obtain optimum sensitivity. Dnce accustomed to using the metar, one can proceed to provide a calibrated

scale for the variable capacitor C3. For this, the gate dipper is used as an AM damodulator. A length of wira (minimum 10 metras) which can be positioned either horizontally or vartically is used as an aerial. The latter is coupled to the coil of the grid-dip meter via a singla-turn coil (see figura 7). One end of the coupling coil should be earthed (to for example a water pipa (etc.). Capacitor C3 is then adjusted until a known AM station can be heard via the haadphones. The oscillator frequency will than be the same as the carrier wave frequency of the transmitter. The scala for the variable capacitor can be calibrated simply by tuning into a number of different stations. If desirad, higher frequencias can be calibrated by amploying a number of tuned circuits of known resonant fraquency. The position of P1 at which reception is the strongest corresponds to the position which gives maximum sensitivity when using the circuit as a grid-dip meter. To facilitate tuning, it is racommended that a tuning capacitor with slow motion drive be used.

Table

kHz
kHz
kHz
kHz
MHz
MHz
MHz
MHz



Although the device described here is called a strain gauge, it is in fact being used to measure stress, i.e. the forces which are applied to it. Strain denotes the deformation of a material (change in form or bulk) as a result of the action of stress. However in ell elastic materiels (such as e.g. steel) there is a linear relationship between stress and strain, which is expressed by the following equation: $\delta = \epsilon$. E, where δ is the strass. e. is the strain, and E is a coefficient termed the modulus of elasticity. Every elestic material has its own modulus of elasticity which remains constent within cartain limits of stress. Since strain is proportional to stress, it is thus possible to measure the one via the other. The basic design of the strain gauge is

shown in figure 1. An electrical signel is derived from a transducer. This signel is then amplified end used to drive an LED scale display. If one looks ahead to figure 3 it can be seen that the electronics involved ere in fact extremely simple. The heart of the strain gauge is the stress ebsorber, the object upon which the forces to be measured actually act, and whose strain is measured. This part of the device cannot be bought, end must be made oneself.

Stress absorber

As is apparent from figure 2, the object which bears the brunt of the forces to he measured is formed from a sheet of suitable matal, with a hole drilled in each end. The central portion is made narrower than the top and bottom, since it is at this point that the daformation of the metal is measured.

The amount of strain is actually measured by a special type of transducer called an electric resistance strein gauge. In its simplest form it consists of a grid of resistence wire cemented between two sheets of paper. The gauge is bonded to the metal, so that it undergoes the seme deformations. The resultant changes in the length and cross-sectional area of the wire causes e proportional change in its resistance.

As figure 2 makes clear, four resistance strain gauges are mounted in a bridge configuration, two on the front of the stress absorber and two on the back. The changes in the resistance of the W. ven Dreumel

There ere few projects which have not formed the subject of an erticle in Elektor et one time or enother, however a strain gauge falls into that category. This in

itself is perhaps slightly surprising. since there are a number of possible applications for such a device - e training aid for 'strength sports', measuring loads on cables, etc, or simple weighing purposes.

vertically oriented gauges (R2 and R3) ara summed, whilst the horizontally oriented gauges provide temperature compensation. A further advantage of this arrangement is that flexing of the metal in the leteral plane will have no effect, since the bridge remains in equilibrium.

The bridge is provide with a stebilised supply voltage. A current of roughly 20 mA can flow through the strain gauges, and since they have a resistance of approximately 120 Ω , the voltage across the bridge is fixed at roughly 5 V.

Circuit

sion

The circuit of the strein gauge is shown in figure 3, and, as has already been mentioned, is fairly modest in dimen-

The low level output voltage of the measuring bridge must be considerably emplified before it can be displeyed, This is performed by two 747 ICs, each of which contains two 741 type op-amps lit is of course also possible to employ four conventional 741's). A1 and B1 are connected as unity-gain amplifiers with high input impedence, so that the bridge is not loaded by the amplifier circuit. The latter is formed by A2 and 82, which ere connected as a differential amplifier with a gain of approximately 1000, adjustable by means of P2. Under quiescent conditions (no force applied to the gauge), P1 is adjusted for zero output voltage.

The display takes the form of a column of LEDs, which are driven by the well-known UAA 170 LED voltmeter IC. Depending upon the input voltage, this chip lights one of the LEDs D3 . . . D18. The input is protected against negative and excessively large positive voltages by zener diode D2.

The power supply circuit is also quita streightforward. Two integrated voltage regulators (7812 and 7912) provide the + and -12 V rails, whilst the 5 V for the resistance bridge is obtained by the inclusion of two resistors (R9, R10) and a zenar diode (D1).

Construction

The amplifier, display driver and displays can easily be mounted on a strip of

Veroboard, or similar. The stress ab sorber, however, is slightly more complicated, since it involves a certain amount of mechanical handiwork,

The dimensions of the stress absorber will depend upon the type of material used and upon the desired measurement range, To obtain optimum sensitivity, the material should undergo as great a deformation as possible when under maximum load conditions. As can be seen from column 3 of table 1, the most suitable material from this point of view is hard brass, with duraluminium a good second. Column 2 of the table is used to calculate the cross-sectional area of the stress ebsorber (X x Y in figure 2). This is done by dividing the maximum permissible stress into the required range of forces to be measured.

The ratio of X to Y can be chosen individually, however X should not be smaller than approximately 10 mm (because of the size of the strain gauges) and the overall shape of the stress absorber should remain similar to that shown in figure 2. The values of R6 and P2 in the circuit diagram are calculated on the basis of a strass absorber made of duraluminium and with e cross-sectional area of 20 mm²

Although electric-resistance strain gauges

are not widely used by the amateur, various types are available commercially. For this perticular application their dimensions should be in the region of 5 x 10 mm. Suitable types are (among others) the EA-XX-250BG-120 from Micro Measuraments, the 3/120 LY 11 from HBM, and the PR9833 k/01 from Philips.

Calibration

10 18 le Under zaro load conditions P1 is adjusted such that the first LED in the scale lights up. A known waight is then suspended from the gauge and P2

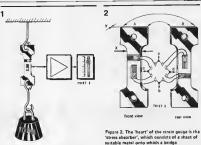


Figure 1. Basic principle of the strein gauge.

Teble 1.

configuration of four electric-resistence street sensors are bonded.

	modulus of elesticity E; kg/mm²	maximum permissible strass 8; kg/mm²	strain, e, a + maximum permiss stress: %
hard brass	9000	42	0.46
dureluminium	7000	26	0.37
semi-hard bress	9000	24	0.27
herd aluminium	7000	14	0.20
sheet steel	21000	18	0.09

Table 1. The information contained in the table allows the suitability of various metals to be assessed, and the cross-sectional area of the 'stress absorber' to be calculated in each case.

adjusted until the corresponding LED lights up (obviously this will depend upon the measurement ranga chosen). If, for example, 10-turn potentiometers are used for P1 and P2, a fairly accurate scale can be obtained. For e variety of raasons, it is possible that the zero point of the scale may tend to fluctuate.

However if P1 is mounted such that it Is accessible externally, this should not presant too many problems.

Literature:

Linear Applications, National Elektor 12, April 1976.

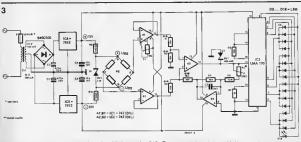


Figure 3. The amplifier and display circuit consists of little more than 3 iCs. The symmetrical supply is provided by two voltage regulator ICs, whilst a couple of resistors and a zener diode provide the 5 V for the measurement bridge,

It is interesting to note that, by and large, our readers' comments and gueries - yes, end problems, too - run parellel to our own, It is even more interesting that ell our problems have been solved, as will be described.

To make full use of a microprocessor, one should normally have access to the instruction menual. For the 2650, this is a 174-page book . . . Fortunately, the main points can be summarised rather more briefly.

specifying negative numbers means that 00...3F are positive; 40...7F are negetive; greater than 7F don't exist. All this mey or may not seem simple in

theory; in practice it has proved a source of endless programming errors . . . easier to miscalculate a relative address than to get it right! For simple progrems, one may es well use 'ebsolute addressing' - the additional memory spece required (the corresponding instructions are longer) is rarely a problem.

I played TV games..

Everything you want to know about making software for the TV games computer, in two easy lessons . . .

In Flektor 48 April 1979, we described how to build a

'TV games computer', Included was a brief explanation of how it works: the 'instructions for use' consisted of little more than the Reed Cassette routine, so that the progrems given on ESS records can be entered.

Apparently, however, the majority of our readers want more: they went to do their own progremming. 'This will prove relatively easy', we said - end to prove it, the (sometimes fairly sophisticated) programs on the second ESS record for the TV Gemes computer were developed by e novice. The following erticle is based on the experience gained . . .

Addressing modes

When fetching or storing deta, or jumping to end fro in a progrem, it is essential to specify the 'eddress' concerned, Obviously. In the TV Games computer, there ere severel different weys of doing this.

Absolute or relative

An 'ebsolute' address is simply the address itself. For instance, in machine language the instruction for 'Load Absolute into register zero' sterts with ØC (more on this later!); if the deta is to be fetched from address @F@O. the full instruction will therefore be @C@F@Ø. A 'relative' eddress, on the other hend. specifies e smell jump in the program. Basically, the processor will celculate an 'ebsolute' address by adding the specified number (between -64 end +63) to the eddress that follows that particular instruction. As en example, if the instruction 'Load Relative into register zero, 2F' (in machine lenguage: Ø82F) is located at the two address bytes 993E and 893F, the following address is 8949. The 'ebsolute' address corresponding to

The negative number required for a 'backwards' jump is entered as a '7-bit two's complement number'. In simple language, this meens that you count down from 80HEX. For instence, if in the previous example the data was to be loaded from eddress #93D, the relative eddress would be 7D: the 'following address', 0940 corresponds to 80, so 093F corresponds to 7F, 093E to 7E and @93D to 7D. The full instruction is therefora: 087D. Note that this way of

this instruction is therefore 0940 + 2F =

096F, and the date will be fetched from

However, practice makes perfect, and as programs get more complex it becomes worthwhile to stert using relative eddresses wherever possible. As an eid to the beginner, one of the progrems on the new ESS record contains a celculetion routine for relative addresses - e useful check!



Oirect or indirect

The two types of addressing explained above are both referred to as 'direct' address modes: data is transferred from or to the specified address. An elternative possibility is a two-step operation: specify en address where the desired eddress can be found. This is referred to as 'indirect' addressing.

Although both absolute and relative indirect eddresses ere possible, only the latter are useful in the besic TV games computer. A relative address is converted to an indirect relative address by edding 80. In the example given above, the 'load relative' instruction @82F was located at eddresses 093E and 093F; the deta was then fetched from eddrass 096F. However, if the instruction is modified to 08AF (2F + 80 = AF) the

Table A.

*****	04 00 50		`
08F0	C# 6# 5# 6)
Ø8F4	3D CE 50 6		DATA
#8F8	CØ ØØ 2B I	F	- DATE
@BFC	63 FE 00 0	10	,
0900	7620	PPSU, II)
0902	05C3	LDDI, R1	1
@9@4	0400	LDDI. RØ	clear PVI
0906	CD5F00	STRA, I-R1	
0909	597B	BRNR, R1)
@9@B	050E	LDDI, R1	1
#90D	-> 0D4BF0	LDDA, I-R1	store
0910	CD7F80	STRA, I/R1	object
0913	597B	BRNR, R1	shape
Ø915	9491	LDDI, RØ) .
Ø917	CC1FC0	STRA, RØ	size
Ø91A	0400	LDDI, RØ	í
Ø91C	CC1FC1	STRA, RO	colour*
091 F	→ 0C1 EBB	LDDA, RØ	4
0922	F420	TMI, RØ	west for
			'PC' key
0924	9879	BCFR	
0026	3FØ5CD	BSTA, UN	save stetus and
4929	1 FGG14	RCTA UN	return to monitor

- As things stend, these two instructions are unnecessary: the data in address FEC1 is stready @6 effer the 'clear PVI' routine. However, other colours can now be selected by modifying the data in the LODI instruction.
- ** This slightly extended 'return to monitor' routine cures the problem of unwanted black squares down the left-hand edge of the screen (see text).

Table A. An illustration of what can be achieved with the instructions described in this article! The program is started at address 6940. If it works, proceed to Table BI

contents of addresses 096F and 0970 will be used as the absolute address for this instruction: If the data stored at these eddresses is 0A and 00, say, the load indirect relative, 2F' instruction will be cerried out as if it read "load absolute from 0A00".

Once again, for simple programs it is

easier, quicker and more reliable to use the corresponding absolute 'instruction, and forget about the 'relative Indirect mode. As en aid to courageous novices, the calculation routine mentioned above extrally gives two results: If the relative jump in the previous examples is calculated, the ensaver will eppear as '2F Or AF' – for direct and indirect, respect-lively!

Indexed

n

In contrast to the "relative" and "indirect" dedressing modes, "indexed" addressing can prove extremely useful in even the simplest of programs. The basic idea is that the data stored in one of the registers is edded to a specified "baso lute" address; the result of this addition is used as the absolute address for the instruction. The register containing the additional data for the address is referred additional data for the address is referred to the containing the

To specify the basic indexing mode, 6040 is added to the absolute address. Thus 905900 is not interpreted as load register one from absolute address 6900°; if we assume that the deta already in register one is 6A, the instruction will be read as Tood register zero from absolute address 9904 ~ i.e. from



9909 plus the data in register one. Two further extensions of this instruction make it invaluable: "Indexed with auto-increment" and "Indexed with auto-decrement", specified by adding 2000 or 4000 to the absolute address. In both cases, the final address is calculated in the same way – by adding the data in the "index register" to the specified

absolute address. However, before calculating the final address, the data in the index register are increased by one ('euto-increment') or one is subtracted from the data ('euto-decrement').

The value of this instruction is best The value of this instruction is best used to the value of the value of the value of the thet we want to clear all "background data" in the PU. This means storing 48 in all flasted of using 45 individual store absolute' instructions, a single store absolute, indexed with eutodecrement' instruction can be used, with a bit of pedding:

The 'shorthend ebbrevietions' given efter the actual machine-code instructions are referred to as 'mnemonics'. They are simply a quick way to jot down what the instruction does.

This brief section of program is executed es follows. First, the 'index register', R1, is loaded ('LODI, R1' = Load Immediate, Register 1 - more on this leter) and '00' is loaded into Register 0. This is followed by the 'Store Absolute, Indexed to Register 1 with auto-decrement' instruction - incidentally, the velue of mnemonics is clearly illustrated here: it is a lot quicker to write 'STRA, I-R1' then the mouthfull given above. At this point, the value in R1 (2D) is reduced by one and the result (2C) is added to the basic ebsol ** eddress 1F80 (5F80 = 1F80 + 4000 for 'autodecrement'). The value in RØ (ØØ) is then stored in the resultant absolute eddress: 1F8Ø + 2C = 1FAC. One down. 44 to go! The next instruction, which will be explained in greater detail leter. is 'Branch if Register 1 is Non-zero. Relative'. Since R1 is most definitely non-zero (it is still 2C at this point), the 'relative brench' is executed: the program 'jumps back' to the beginning of the previous instruction, as indicated by the arrow. This whole performance is repeated, storing 00 in progressively lower PVI addresses, until the data in

Teble 1.

Ø9Ø3	954E 9499	LDDI, R1 LDDI, R6	1	
0907	CD5F99	STRA, I-R1	- (clear objects
090A	□ 597B	BRNR, R1)	
090C			Ĵ	colour
			1	colour
			1	
			(background
			(Down ground
			}	
091A	40	HALT*	/	
	0905 0907 090A	0905 0400 0907 05509 0906 0469 0901 0520 0413 04FF 0918 0578	9985 0400 LDDI, R0 9987 CD5F90 STRA, FR1 9980 0469 LDDI, R0 999E CC1FCS STRA, R0 9911 052D LDDI, R1 9913 04FF80 STRA, R0 9915 CD5F80 STRA, R0 9916 E978 BRNR, R1	9985 0400 LDDI,R0 9987 CD5F90 STRA,FR1 9980 0469 LDDI,R0 9991 0520 LDDI,R1 9913 04F80 STRA,R0 9915 CD5F80 STRA,R1 1 9918 5978 BRNR,R1

Not the bast way to end e progrem, as we shall see, but good enough for now!

R1 becomes zero. At this point, the BRNR, R1, instruction does not result in a jump back, since R1 is zero, and the rest of the program is carried out.

For those who feel like trying out this program, it is more interesting to turn the background on instead of off, in that case, the background and screen colour must also be specified: '89' in address 1F06 gives yellow on blue. Furthermore, the objects will have to be cleared, since they are also used by the monitor program. A complete program is given in Table 1; the rescon for starting at address (993) (instead of 9940) will

be given later.
While on the subject of indaxed addressing, one final point should be noted. In general, this mode is available as a variation of all absoluta addresses, with the exception of branch instructions. The only two indexed branch instructions, BXA and BSXA, will be discussed further on.

To or from register (zero)

Naarly ell instructions involving trensfer or manipulation of data require the use of a register. Obviously, the register to be used must be specified in the instruction.

In the axemples alraxdy given, and Table 1 in particular, this principle is clear. The first byte of each instruction specifies the basic instruction and the register involved. For instance, the basic instruction for 'Load Immediate' is @4xx (whare 'xx' is the data to be loaded); adding the number of the



Table B.

The program given in table A should produce a white object on a blue screen. To include a

"background"	, the program can b	@ modified from	acidress @91F on, as foll
(Ø91C	CC1FC1		1
@9tF	9489	LODI, RØ	
9921	CC1F91	STRA, RO	1
0924	CC1F93	STRA, RØ	
0927	CC1F9F	STRA, RØ	
0 92A	CCtFAt	STRA, RO	load
0 92D	049C	LODI, RØ	background
092F	CC1F98	STRA, RO	Dackground
0932	9439	LODI, RØ	1
0934	CC1 F99	STRA, RØ	
0937	0401	LODI, RØ	1
0939	CC1FA8	STRA, RO)
Ø93C	0449	LODI, RO	colour
@93E	CC1FC6	STRA, RO	Colour
Ø941	→ 0C1E88	LODA, RO	wait for
0944	F420	TMI, RQ	'PC' key
0946	9879	8CFR) PC KEY
Q 948	3FØ5CD	8STA, UN	save status and
094B	1F0014	BCTA, UN	feturn to monitor

The complete program is again started from \$999 For the next step, see Table C.



register to this gives the complete instruction: 49xx for Register 9, 45xx for Rel and 97xx for R1, and rel and 47xx for R3, in practice, this means that four variations exist for most instructions: one for aach register. It also means that the second digit in an instruction specifies that register involved: 9, 4, 9 and C for register 0 (8883, for instrucci); 1, 5, 9 and D for register 1; and so on 40 D for register 1; and so on

Finelly, some instructions refer to data transfer or manipulation involving two registers, one of which is always register

zero. The Instruction 'Load Ragister @ from Register 1', for insteamen, is @1. Similerly, 'LODZ, R2' (to use the mnemonic) is @2. It should be noted that in some cases, but not all (1), both registers can be specifiad as Register @. This can somatimes be useful, as will be explained under 'programming tricks', next month.

Registers

We have elready mentioned 'registers' several times. It is now time to take a closer look at them. To put it in a nutshell, a register can be visualised as a memory location inside the microprocessor itself. In the 2650, 8-bit registers ere used; this means that they can store any date value from 60 to FF. In all, seven 'general-purpose' registers ere available: register @ and two 'banks' of three registers (R1, R2, R3 and R1" R2' and R3'). Of thase seven, register & is always immediately available; et any given moment, however, only one of the register benks (R1...R3 or R1'...R3') is accessible. The other bank, and the

Figure 1.

Program Status Word

	PSL	J						
bit:	7	6	5	4	3	2	1	0
function.	S	F	н	Not Used	Not Used	SP2	SP1	SPQ
hex code:	8ø	40	20	10	08	94	02	91

S Sense SP2 Stack Pointer Two F Flag SP1 Stack Pointer One II Interrupt (nhibit SP9 Stack Pointer Zero

vo ne iro PSL 7 6 6 4 3 2 CC1 CCO IDC RS WC OVF COM С 80 49 20 10 08 0.4 02 01

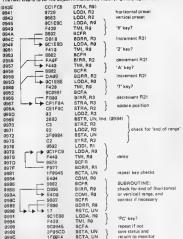
CC1 Condition Code One WC With/Without Carry
CC9 Condition Code Zero OVF Overflow

CC9 Condition Code Zero OVF Or IDC Interdigit Cerry COM Le RS Register Bank Select C Ce

COM Logicel/Arith, Compare C Cerry/Sorrow

Table C.

The program given so far in tables A and 8 will produce a stationary object and background. The next step is to sel the object in motion, by modifying the program from address 9941 on:



After loading this program, it should be possible to move the object to end fro horizontally by operating the '5' and '7' keys; vertical control is provided by the '2' and 'A' keys

data contained in those three registers, is 'in cold storage'. (The way in which one or other of these banks can be selected will be discussed below: see 'Program Status Word'). Any instruction referring to R1, R2 or R3 is performed only on that register in the selected bank—it has no effect on the corresponding register in the other bank.

Program Status Word

The 'Program Status Word' refers to two speciel purpose 8-bit registers: the 'Program Status Upper' (PSU) and 'Program Status Lower' (PSL). Each bit in these registers has a special meaning, as illustrated in figure 1. Briefly, the most important points es they relate to the complete TV games computer are as follows:

 sense: this bit is '1' for the duration of the vertical reset pulse, at the end of each 'frame'. It can be used, for example, to synchronise the program to

the actual display on the screen,
- flag: can be set, reset and tested et

will, as an indication of some condition relating to the program – for instance, to distinguish between the first and following runs through a particular section in the program. – Interrupt Inhibit. The PVI generates

— Interrupt Intibit. The PVI generates interrupts at the end of each frame and each-time an object is completed. If this bit is set, these interrupt requests are ignored; otherwise, program execution "jumps" from wherever it happens to be to address 6983 and runs the program section that it finds there as a subroutine. Note that this can cause as subroutine. Note that this can cause



Sreck pointers. These three bits are set and raset by the processor, to keep track of the "subroutine levels". The stack is eight levels deep, which means that the main program mey branch to a further subroutine, the may branch to a further subroutine, and so on but only times before starting to climb back up to present the program of the program of the program of the program of the program. But this is unwise for program, but this is unwise for beginners.

- Condition Code, These two bits are set by (the results of) several different instructions, as shown in the Instruction Set given elsewhere. For instance, if the data loaded into a register is 00, the condition code will elso be set to 00. Most of the branch and return instructions can be made 'conditional', by specifying a particular condition code setting: in that case, e 'Brench on True' instruction, for Condition instance, will only be executed if the actual condition code at that point corresponds to the one specified. If the two don't correspond, the instruction is ignored.

 IOC, WC, OVF, COM, C. These five bits will be dealt with later; see: Arithmetic and Compare.

- Register bank Select. This bit is used



Table 2. Lord and Store

description

Load register zero
Load immadiate
Load relative
Load absolute
Store register zero
Store seletive
(STR2)
Store stoplute
(STRA)

and and atom

example
02
04*x
08yy
0Czzzz
C1
C5yy

CCzzzz

don't axist.

data 'CA' into register 3.

addressing is required.

comments

from R2 to R0
'xx' = data
'yy' = displacement
'zzzz' = address
Io R1 from R0
'yy' = displacement
'zzzz' = address

main program: the main program is stopped at the branch-to-subroutine instruction, the subroutine (elsewhere in memory) is carried out, after which the main program continues at the point where it was interrupted, Several variations of both types of Branch instruction are available:

Branch (to Subroutine) on Condition True, Relative or Absolute, For each of these four basic instructions, a particular setting of the Condition Code bits can be specified; the branch will only be executed if the actual condition code corresponds to the one specified, For example, the basic instruction for Branch on Condition True, Absolute (BCTA) is '1Czzzz', where zzzz is the absolute addrass to which we want to jump. As it stands, this branch instruction will only be carried out if the condition code is 00. Similarly '1Dzzzz' end '1Ezzzz' specify the condition codes @1 and 10, respectively. Finally, '1Fzzzz' would seem to rafer to a condition coda 11, but this code doesn't exist. In fact the corresponding instruction is used for an unconditional branch: a branch that is elweys carried out, no matter what the

Branch (to Subroutine) on Condition False, Relative or Absolute. These four instructions are similar to those described above; the only difference is thet the branch is executed if the acute condition code does not correspond to the one specified. The "BSFA" instruction BCZEZZ, for example, will cause a specified. The "BSFA" instruction BCZEZZ, for example, will cause a code is either 61 or 18, but not ril it is 90. Note that no 'unconditional' variations of these instructions exist: the corresponding codes 9Byy, 9FzZZZ are used for other BByy and BFZZZZ are used for other

condition code.

instructions.



of the other three registers. 'C1', for

example, trensfers deta from RØ to R1.

Note that the instructions '00' and

'CO', for 'LODZ, RO' and 'STRZ, RO',

Load immediate transfers the data given

in the instruction to the specified register. '07CA' (= LODI, R3) loads the

Load relative and Store relative refer to the relative addressing mode described

aarlier. Relative Indirect addressing can

used when ebsolute or absolute indexed

also be used, as described parlier,



to select one or other of the two 'register banks' described above.

Various manipulations are possible on the two Program Status registers, es will be described. The Clear, Prases and Test these are the combination of this to 9 or 1, as combination of bits to 9 or 1, as required, end to test the satting of any bits], An example was given abova: bits], An example was given abova: Status, Uppar, Masked 26'; as can be seen in figure 1, this sets the Interrupt Inhibit bit.

Instruction Set

Severel instructions have already been mentioned briafly; having laid the groundwork, it is now possible to examina the instruction set in greater detail.

Load and stora

The principle of these instructions is obvious: data is transferred into (Load) or from (Store) a specified register. Load Register zero and Store Register

Load Register zero and Store Register zero transfer data between RØ and one



In ell cases, the two Condition Code bits are sat according to the sign of the date transferred: they become \$1 if the data is a positive number, \$00 if it is zero and 10 if it is negative (i.e. \$9...FF, corresponding to \$-128...-1). The Loed and Store instructions can be summarised as shown in Table 2.

(Subroutine) Branch

Normally speaking, a program is executed stap by step: in other words, the instructions are carried out in the order in which they are stored in the memory. If a jump to a different section of the program is required, a so-called Branch instruction must be used.

Thara are two besic types of Brench instruction: those for a (main program) Branch and those for a Branch to Subroutine. In the former case, the main program itself jumps to a different point in the memory; a Branch to Subroutine, on the other hand, can be considered as an interruption in the



Branch (10 Subroutine) on Register Mon-Zero, Raletive or Absolute, Au part of these instructions, one of the register (RB ... RB) is specified. If the content of this register is not zero, the branch instruction is carried out otherwise it is ignored. 'BRNA, 'RB' (\$Czzzz), for instance, will easie e jump to addrass zzzz provided tha data stored in Register (8 is not zero.

Branch on Incrementing (Decrementing) Register, Relative or Absoluta. These instructions are an extension of the pravious set. Once egain, a register is description

		_	_
Table 3.	Brench	(to	sub

oble 3.	Brench (to subroutine

Brench:		
On Condition True, Relative	(BCTR)	18yy
On Conditition True, Absolute	(BCTA)	1Czzzz
On Condition False, Relative	(BCFR)	98yy
On Condition False, Absolute	(BCFA)	9Czzzz
On Register Non-zero, Rel.	(BRNR)	58yy
On Register Non-zero, Abs	(BRNA)	6Czzzz
On Incrementing Register, Rel.	(BIRR)	OSyy
On Incrementing Register, Abs.	(BIRA)	OCZZZZ
On Occrementing Register, Rel	(BORR)	FByy
On Occrementing Register, Abs	(BORA)	FCZZZZ
Zero Relative, Unconditional	(ZBRR)	9Вуу
Indexed Absolute, Unconditional	(BXA)	9Fzzzz

Brench to Subroutine:

(BSTR)	38yy
(BSTA)	3Czzzz
(BSFR)	BByv
(BSFA)	BCzzzz
(BSNR)	78yy
(BSNA)	7 Czzzz
(ZBSR)	ВВуу
(BSXA)	BFzzzz
	(BSTA) (BSFA) (BSFA) (BSNA) (BSNA) (ZBSR)

Return from subroutine:

Conditional			(RETC)	-1
And Enable	(nterrupt,	Conditional	(RETE)	3

Program Status

1Byy = unconditional

36yy = unconditional

BByy: see below

BFzzzz: see below

3Fzzzz = unconditional

9Byy: see below

9Fzzzz: see below

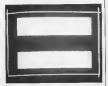
1Fzzzz = unconditione(

comments

R3 only l

The function of the various 'bits' in the Program Status Registers was explained above. At this point, we are only interested in the available instructions (as summarised in Table 4).

The Load and Store instructions refer to data transfer between one of the Program Status Registers and Register @ only, 'Load Program Status Upper' (LPSU: 92) for instance, loads the contents of RØ into the PSU.



In practice, these instructions will not be used often, since in most cases Clear, Masked or Preset, Masked instructions ere more suitable. 'Clear Program Status Upper, Masked 40' (7440) will

comments

from RØ

from RØ

mm = mesk mm = mask

mm = mask

mm = mesk

mm = mask mm = mask

RØ ... R3

to RØ

to Bo

specified. In this case, however, 01 is first added to (increment) or subtracted from (decrement) the contents of the register, after which the branch instruction is only cerried out if the new contents are non-zero. Note that no 'Branch-to-subroutine' version of these instructions exists.

Zero Branch (to Subroutine) Relative, Unconditional. These two instructions are relatively useless in the TV games computer, since they specify a branch relative to address 6000. the start of the monitor program!



Brench (to Subroutine) Indexed. Absolute. Unconditional. These two instructions ere the only two indexed branch instructions that exist. The value in the index register (which must be R3) is added to the basic absolute address given, and the brench is executed to the resultant address.

Return from subroutine, conditional, As before, a condition code is specified as part of this instruction; if the actual condition code matches, the subroutine

Teble 4.

example

Program Status, Test, Compere, etc.

R3 only1

description		exemple
Load Program Status, Upper	(LPSU)	92
Load Program Status, Lower	(LPSL)	93
Store Program Stelus, Upper	(SPSU)	12
Store Progrem Status, Lower	(SPSL)	13
Clear Program Status, Upper, Masked	(CPSU)	74 mm
Clear Progrem Status, Lower, Masked	(CPSL)	75 mm
Preset Program Status, Upper, Masked	(PPSU)	76 mm
Preset Progrem Status, Lower, Masked	(PPSL)	77 mm
Test Program Status, Upper, Masked	(TPSU)	B4mm
Test Program Status, Lower, Masked	(TPSL)	B5mm
Test Under Mask Immediate	(TMI)	F4mm
Compere to Register Zero	(COMZ)	EØ E3

Compare Immediate Compere Relative Compers Absolute

Halt

No Operation

(NOP) CO

(COMI) E4xx . . . E7xx xx = value (COMR) E8yy .. EByy (COMA) ECZZZZ . . . EFZZZZ

, F7mm

(HALT) 40

clear the 'flag' bit, without having any is terminated. An unconditional end of effect on the other bits in the PSU. the subroutine is indicated by the Similarly, 'PPSL, RS' (7710) will select condition code 11, so the instruction RETC, UN is 17. A variation on this the second register bank. instruction exists (RETE) that not only Finally, any bit (or combination of bits)

ends the subroutine, but also resets the Interrupt Inhibit bit. Not a good idea, until one has gained enough experience to start using the interrupt facility . . The complete set of branch instructions is summarised in Table 3.

in each of the program status registers cen be tested: 'Test Program Status Upper, Masked 40' (B440) will cause the Condition Code to be set to 00 if the 'flag' is set; otherwise the Condition Code will become 10.

Table D

09D7

09DA

With the complete program given so far (in tables A ... C), it is possible to get the object into your sights. Now, what about shooting it down?!

First, modify the instruction in address 9962: instead of '909991', enter '90999B'. The existing program, from address 9990 is then extended as follows.

(098E		F800	BORR, RG)		
0990		C0 C0	2 x NDP	1	this leaves
0992		CØ CØ	2 x NDP	1	room for a
9994		C0 C0	2 x NOP	>	section of
0996		OØ CØ	2 x NDP	l	program to be
0998		CO CII	2 x NDP)	added later
099A		17	RETC. UN		
899B		F480	TMI, RØ	1	
099D		8830	BCFR	ì	'F' kay?
699F	/	7702	PPSL, CDM	1	horszontal
@9A1	/	E756	CDMI, R3	1	co-ordinata
09A3		992A	BCFR	?	between
09A5	//	E75B	CDMI, R3	į.	67 and 5A?
09A7	r	9A26	BCFR)	
@9A9	/ i	E6B1	CDMI, R2	1	vertical
09AB	I 1	9922	BCFR	1	co-ordinata
@9AD	1/ i	E686	CDMI, R2	>	between
89AF	ľ !	BA1E	BCFR	1	82 and 85?
Ø9B1	1/	150A	LDDI. R1	<	
0 983		ID49A8	LODA, I-R1	1	stora random
0 986	1 1	CD7FGG	STRA, I/R1	?	date in
Ø989		5978	BRNR, RI	1	object shape
8988		9564	LDDI, R1	ζ.	
@9BD		C1FCB	LODA, RO	1	
09C0		F440	TMI, RØ	5	dalay
09C2		987B	8CFR	1	
09C4		FB77	8DRR, R1)	
09C6		Ca Ca	2 x NDP	`	
Ø9CB		CØ CØ	2 x NDP	1	leaving some
89CA		00 00	2 x NOP		more reom
Becc		1 F@9@@	BCTA, UN	-	repeat from 0900
89CF		C1 E88	LDDA, RØ	1	
89 D2		F420	TMI. RØ	}	'PC' key?
09D4		RC8945	BCFA	1	repeat if not

BSTA. UN BCTA, UN Once the object is accurately (ii centered, it can now be 'shot to pieces' by operating tha 'F' kay



3F05CD

1F9914

Tast under Mask: Compera

With all the conditional branching facilities available, is is obviously useful to have instructions that set the Condition Code, Basically, all types of data transfer to or data manipulation in a register do this; furthermore, the Test Under Mask Immediate (TMI) and Compere (COM) instructions set the condition code bits without altering the data in any way.

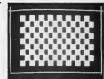
The TMI instruction is the easiest to use: a register is specified in the first part of the instruction ('F4' for register zero.



sme status and

ratura to monitor





The compare instruction is basically similar, but it is both more precise and more versatile - and also more complicated to use. In this case, a data value is specified insteed of e mask, and the condition code can be set in three weys: Ø1 for 'greater than', ØØ for 'equels' and 10 for 'less then'. There are two main points to watch, when using this instruction: what is meant by 'greater then' (data in register greater than data specified, or vice versa; see the footnotes in the Instruction Set) and what type of comparison is required. With the 'COM bit' in the PSL set to Ø, an 'arithmetical' comparison will be performed; all values from 80 to FF are treated as negative numbers (two's complement) If the COM bit is set to 1 (by meens of the instruction 7702 = PPSL, COM) a 'logical' comparison will result: the date is treated as a positive 8-bit binary number



No Operation

A surprisingly useful instruction, this! When the processor finds the code 'CO' it simply carries on to the next instruction. There ere two cases where this can be particularly useful: to 'delete' instructions that prove unnecessary, without having to re-enter the rest of the program, and to 'leave a gap' into which further instructions are to be edded at a later date.

This stops the processor, quite drastically. The only way to start it up again is either to operate the 'resat' key or provide an interrupt - provided the interrupt inhibit bit is not set. In general, this is not a good idea; in the TV games computer, a 'return to Monitor' instruction (1F0000 = BCTA, UN, for instance) will usually be mora suitable.

A few tips

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The instructions explained so far are sufficient for simple programs. The remaining fecilities will be dealt with next month. Meanwhile, however, a few prectical tips on how to program should

prove useful. First and foremost: remember to block the Interrupt facility if this is not required in the progrem! For the time being, it is advisable to start every progrem with the instruction "7620"

(PPSU, II). There are several ways to end a program. Usually, one of the keys ('PC', for Instance) is used to initiate a jump back to Monitor, A few verietions are given at the end of Tebles A. . . O. The jump to Monitor itself can be done in several ways. The shortest is to use a ZBRR instruction: '9880' should do the trick, but we've never actually tried it. A



similar solution is "1F0800", es mentioned earlier; this we have tried, and it usually works. Somatimes, however, for no apparent reason problams occurs in particular, a row of black squares or lines down the left-hand degle of the scream whan the program is restarted. Without knowing why this happens, yet impab as well know more next monthil, we can offer three solutions:

- return to monitor by means of the

0400 LOOI, RG 1F0011 BCTA, UN

Note that, in this case, the original value in RØ is lost; for thet matter, raturning via eddress 0000 always causes the data in RØ to become 09, as several readers here noticed!

9B11 ZBRR This has the advantage that if fits in the same memory spece as '1F0000', if the latter ceuses trouble.

 finally, if the value in RØ is to be stored:

3F05CO BSTA, UN 1F0014 BCTA, UN

Oon't ask us to explein this one — that would require en extensive discussion of the monitor softwere!

When it comes to the program itself, the first thing is to work out what you want to do. Obviously. For simple programs, this can usuelly be put into words quite

Teble 5.



Teble 6.



easily. The program givan in Table 1, for example, was originally specified as 'clear objects' define background colour;' lode FF in all background bytes'. For more complicated programs, some more extensive edvance plotting may be required —using a flow chart, say — but usually a complicated program can be 'broken up' into several simple routines. These can each be tried and tested individually, before 'tecking tham together' to obtain the complete final

program.

As each semi-complete routine is entered, it is highly edivisible to store it on tape before the first test run. This lesson was learned the hard way, when one misplaced relative eddress caused 'garbage' to be stored at all sorts of wakward places throughout the program. The only solution was to laboriously re-enter the whole program.

When it comes to 'de-bugging' a program—it always does, no program works perfectly first time!—the 'Breakpoint' routine can be vary useful. There are two points to watch, however. In the first place, as mentioned in the original articla, the Breakpoint address of an instruction. For instance, in the following section of program:

0900	7620	PPSU, II	
0902	0400	LOOI, RØ	
0904	0605	LODI, R2	

breakpoints can be specified at eddresses 98908, 9992 on 6994, but no re 6994, but no et 6994,

The PVI and keyboard

The mein points regarding the PVI were



9A91

Finally, what about edding a time limit? As follows:

- first, fill in the space in the program starting at address \$990:

(098E	F800	BDAR, R9)
0990	7710	PPSL, RS
Ø992	E700	COMI, R3
0994	9802	BCFR
0996	9709	LODI, R3
0999	→ 7510	CPSL, RS
	, fill in the space st	arting at 09C6:
(Ø9C4	F977	BDAR, R1)
Ø9C6	7710	PPSL, RS
Ø9C8	0700	LODI, R3
Ø9CA	7510	CPS) BS

set the 'clock' (R3 in the upper register bank) going as soon as the object is first moved

the object is his modify the date at address 9991: instead of '1F9945', the instruction becomes '1F99DD'

at address 99D4, the instruction is modified to '90976' linstead of 909945).

BSTA. UN

the program is extended, from address 99DD on, as follows: (09DA 150014 BCTA, UN) 09DD 7710 PPSL, RS 09DF E700 CDMI, R3 09F1 9804 BCFR 09E3 0619 LODI, R2 09E5 1B@B BCTR, UN 09E7 ▶ CF1FC9 STRA, R3 **GREA** FA96 BDAA, R2 MOFIC 0610 LODI, 82 d9EE FR02 BDRR, R3 09F0 1805 BCTR, UN 09F2 → 7510 CPSL, RS 09F4 1F0945 BSTA, UN 09F7 CF1FC9 STRA, R3 ODEA 04FF LODI, RO 09FC CC1 FC6 STRA RO 09FF 7510 CPSL, RS

1F09BB

if 'clock' stopped (R3' = QQ). preset R2' for one-second count

update score and decrement R21 reset R2' end decrement R31 brench if R3' = @@ repeat key check routing

set R3' to zero when

store 99 in score, meke screen white ('you lose'l) and repeat via dalay routine



ell discussed in the original articles and

the data supplied with the p.c. board.

One point, however, did not receive all

the attention it deserves - at the time.

given in Table 5. Basically, what happens

is that the processor waits until it finds VRLE = 1; it then decrements the value

in R2 and repeats the VRLE scan if R2

is not yet zero. The result is a delay

approximately equal to the value in R2

times the frame period (20 ms), 8y way

we didn't realise how useful it was! The 'VRLE' bit, at eddress 1FC8, goes high at the end of each frame; it is reset at the end of the VRST pulse or when read. This means that it can only be read as '1' once for each frame. As an example, a simple 'delay' routine is of demonstration, this routine can be included inside the 'load background' loop in Table 1. The result is given in Table 6

Finally, the keyboard, Each column corrasponds to one eddress; 1E88 for the column above the '-' kay, 1E89 and 1E8A for the next two columns, 1E88 for the column that includes the 'reset' key (note that this key itself is not



scanned in the kayboard layout suggested!) and 1E8C . . . 1E8E for the last three columns. When reading the keyboard in this way, the four left hand bits retrieved as data correspond to the four keys in the column - and the other four bits are all ones! '1F' at address 1E88, for instance, means that the



'-' key is operated; '4F' at 1E8A at corresponds to key '8'. Note that me contact bounce can sometimes be a w problem with this type of rapid h key-scan. A more sophisticated routina, in using part of the Monitor software, will in be described next month.

RCAS, WCAS and ESS

The Cassette routines were discussed in the earlier articles. Apparently, some readers have hed problems loading the first ESS record, so a few words of advice may be appreciated . .

Assuming that a cassatte recorder is used, the first point to check is that programs can be stored on tape from the computer and retrieved without any problems. This can be done without even loading a program: there is always soma kind of data in the memory! The test sequence is as follows:

- operate the 'reset' key; - operate the 'start' key ('IIII' should

appear);

- press the 'WCAS' key ('bEG ='): enter 0900 followed by

('bEG = 0900, End = '); OFFF, followed enter

('End = ØFFF, SAd ='): enter 0900, followed

('SAd = 0900, FIL ='); enter 1, but not '+' ('FIL = 1'):

- start the tape in the Record mode.

and set the level to about half way: operate the '+' key.

Hopefully, the recording leval meter should indicate approximately nominal full modulation during the first second or so after the '+' key is operated; it will then drop back slightly (to a few d8 below full modulation). If this is not the case, the level setting can be corrected, after which the whole sequence described above will have to be repeated. Having found the correct level, it is wise to make a note of it, for future reference.



Having made a complete recording at correct level, the various addresses entered above will reappear on the screen. The test can now be concluded:

— operate the 'RCAS' key ("FIL=");
— enter the file number, "1" ("FIL=1");

- press the '-' key (not '+'7).

The text "Fil.—1" will jump to the top of the screen. The tape can now be played back, and the date recorded on it will be compared with the original data in the mamory. During this time (approximately 35 seconds) two dots will flash below the "--" sign on the caproximately 45 second, the end of this time, all the to cripinal data will reappear on the screen as with the added line "CE = 900%! If this dispapear, all is well and the cassette interface is working.

In the unhoped-for event that the check

routine breaks off before the end of the recording, with the message 'Ad= 090A', for instance, then something is wrong... In our experience, moving the recorder further away from the TV set invariably curses the problem.

bother in problem. Next step. The ESS record. You would axpect that recording it on tipe and the problem. The problem is not provided in the computer should be proposed in the computer should be proposed in the computer of the proposed in the computer step. The program for no apperant reason. (Message: "Ad = ..."). Since the exception of the missing "Interrupt Inhibit" instruction in file 6, as mentioned earlier) it must be possible to load them, In one perticularly stubborn case, the following solution was found.

R LITTLE
FrACTICE
dOES
H LOT OF
GUOD
::::::

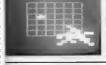


Table 7.

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B e l,

9900	7629	PPSU, II	
0902	3F9161	BSTA, UN	(clear/initiate PVI)
0905	9639	LDDI, R2	
0907	→ 0508	LODI, R1	
0909	→ @E492D	LDDA, I-R2	(cinta)
090C	CD4890	STRA, I-R1	
090F	5978	8 RNR, R1	
0911	7710	PPSL, RS	
0913	3F020E	BSTA, UN	(losd MLINE)
8916	7510	CPSL, RS	
0918	- SAGA	8 RNR, R2)	
091A	→ @C1E89	LDDA, RØ	weit for
Ø91D	F410	TMI, RØ ('+' key
Ø91F	→ 1879	BCTR /	release
0921	1F0038	BCTA, UN	return to monitor
8924	→7710	PPSL, RS	
9926	3F@2CF	BSTA, UN	(scroll)
0929	7510	CPSL, RS	
0938	1B5A	BCTR, UN	

#92D	17 A2 A2 A2 A2 A2 A2 A7 sixth line)
9 935	17 17 19 09 09 00 17 17 fifth line	
Ø93D	9A 17 11 99 8C 17 99 9F fourth line	DATA
0945	17 17 9D 00 0E 05 17 17 third line	CUATA
@94D	14 15 GA GC BC 12 GC GE second line	
@955	QA 17 11 12 BC BC 11 QE first line	/

Just to what the appetite: the gimmicks used in this program will be discussed next month! The start address is 9999.

the tone and volume controls, is fed to the TV games computer. A 'high' file number is entered (8 or 9) in the RCAS mode, and the record is started. After some menipulations with the volume control, two dots will start to flash repidly under the '=' sign, and the actual file number should also appear on the screen. The trick is now to manipulete the volume control (and, if necessary, the treble control) until the dots flesh regularly and the second file number remains constant for the duration of each program on the tape. Once this is achieved, the volume and treble controls are left strictly alone and each program in turn is loaded into the computer (this should work, now) and from there to the tape. From now on, the programs can be retrieved reliably from this tape. Rest assured, we are doing our utmost to make the second ESS record for the TV games computer easier to load . . .

ESS 006

... the second record with software for the TV games computer, which is what this erticle was to have been about.

However, it's long enough as it is. Some idea of the programs can be obtained from the photo's distributed liberally throughout these pages. One program converts the computer into a fairly comprehensive colour TV test pettern generator; the other can be considered as a programming eid. It contains routines for composing object shapes end background on the screen - so that you can see what you're doing -, the 'reletive address calculation' mentioned earlier, and a routine for scanning a charecter set available in the monitor program as will be explained next month.

Full details of how to use these progrems will be included with the record, which will be made available next month.

In conclusion

With the information given in this erticle, it is possible to write simple programs. Some examples are included on these pages. Now is the time to start practicing - next month we'll discuss the rest of the instruction set, and give some rather more complicated routines... After that, you will know as much as we do!



There are a variety of different ways in which the control voltages can be programmed and stored: e.g. via potantiometers, switches, sample-and-hold or digital memories, The circuits method adopted here is to encode the voltage digitally and store it in a RAM, When the contents of the memory are read out, they are fed to a D/A converter, which provides an analogue signal suitable for faeding to the synthesiser VCOs. In addition to the pitch of the notes (i.e. their frequancy), thair relative length can also be progremmed. The duration of each note can be selected in the ratio of 1:2:4:8. The block diagrem of the progremmable

circuit end the 'subsidiary' address counter, however, even longer (or indeed shorter) sequences ere also possible. The note length is controlled by a D/A converter and VCO, the output of which varies the clock frequency of the main address counter. The analogue voltages from output A ere fed to the synthesiser VCOs; at output B e gate pulse is generated to eccompany each note. The gate pulse, whose width can be varied, is used to determine the start and duration of the envelope control voltage generated by the ADSR module of the synthesiser, The complete circuit diagram of the programmable sequencer is shown in

programmable sequencer

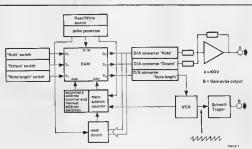
Sequencers are extremely popular add-on units for music synthesisers. Thay are used to store pre-programmed sequences of control voltages for the synthesiser VCOs/VCFs; the control voltages can be 'palyed back' into the synthesiser, thereby generating note sequences which can be used for example to provide the becking to a menually played melody.

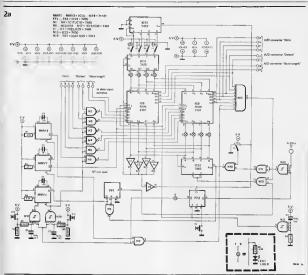
sequencer is shown in figure 1. The pitch (i.e. its position on the musical scele and its octave) and length of the note are set up in binary code on switches which ere connected to the data inputs of the RAM (see figure 3), The address into which the data is storad is determined by an address counter. In actual fact, two address counters are employed, one of which (the 'subsidiary' counter) is clocked by the other ('main' counter). When the stored melody is to be pleved back. the address counter steps through each of the memory locations in turn. The deta is read out and fed to the digital analogue converters, which provide the ectuel control voltages for the VCOs. During normal operation the circuit can store 16 sequences of 16 notes apiece, i.e. a combined sequence of 256 notes; with the eid of the reset figures 2a and 2b, Figure 2a contains the digital section of the sequence, comprising his memory, address counter and reset circuit, whilst figure 2b shows the DIA converters and output stages from 2 (2015, 256 x 4bc) it Rhilst, connect which the digitally encoded control volteges are stored. The higher order dedressed of the input date ers set up on switches 52 ..., S5. The fillipsid (CI11) interposed between the switches and the RAMs ensure that the new address set up on 52 ..., S5. The fillipsid address set up on 52 ..., S5. S s only presented to the address inputs of the RAMs from the previous note sequence.

has ended.

The main address counter is formed by 1610. The counter is clocked, via 106, by the analogue section of the circuit shown in figure 2b. This counter energets the "low order" addresses.

C. Voss





i.e. it clocks from '0000' to '1111', whereupon the high order address is incremented by one (via \$2...\$5), before the counter resets and starts to cycle through another sequence of 16 addresses.

op es

The reset circuit is formad by N12 and N13. When the data outputs a . . . f of the RAM all go high, N12 and N13 ensure that the binary counter is reset to zero. Thus the address containing the data word '111111' represents the reset address, invertes 11 . . . 14 form a NOR gast (the inverters all have open-collector outputs), so that only when the address counter resets (i.e. its outsets that a new high original containers that a new high original containers

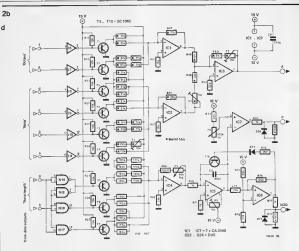
When \$2...\$5 are set to position c, the subsidiary' address counter (IC12) is connected to the address riputs of the RAMs. This counter is clocked by IC10, via 11...15, so that it receives a clock pulse every time IC10 resets (i.e. every 16 addresses). Thus if all the outputs of IC12 are connected to

the RAMs, the entire contents of the memory can be read out in sequence. Switch \$1 determines the operating mode of the sequencer. In position a the switch blocks gate N10, with the result that the address counter is immediately inhibited. In position b the sequencer popularies normally, whilst in position or the counter will stop once it resches '9009."

To actually program a sequence of notes into memory, pushbutton switch S9 is first pressed, resetting the address counter via N12 and enabling the RAMs. The information relating to the pitch and length of the note to be stored is then written into the RAMs by pressing \$10, Each of the monostable multivibrators MMV1 . . . MMV3 are now triggered in turn. The output pulse from MMV1 clocks the address counter (IC10) via N9. The pulse from MMV2 temporarily puts the RAMs into the write mode, so that the information present on the data inputs is in fact stored in memory. The Q output of MMV3 takes the output of N8 high. so that N13 is capable of recognising the reset code ('111111') on the data

outputs of the RAMs.

The next note is written into memory in the same way; the input data is set up on the corresponding switches whereupon S10 is pressed and the data is written into memory Once the desired sequence of notes is stored. pressing S11 writes the reset coda into the memory by taking the inputs of N1...N6 low and hence the data inputs of the RAMs high, When N13 recognisas the reset code, the address counter (IC10) is reset, so that via 11...15. flip-flop FF2 is triggared and the RAMs are returned to the read mode. Schmitt trigger N21 ensures that FF2 assumes a definite state upon switch-on and that the RAMs are inhibited for a brief initial period. The digital-analogue converters and output stages of the circuit are shown in figure 2b. IC1 ... IC3 produce the analogue control voltages which determine the frequency of the notes, whilst the D/A converter round IC4 is used to control the length of the notes. Unlike the other two D/A converters (IC1/IC2), the output voltage increases in an exponential, not linear fashion.



That is to say, when the digital input signal increments by '01', the output voltage doubles.

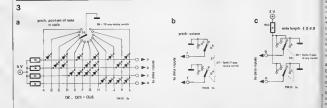
The output of IC4 is fed to a sawtooth

generator formed by IC4 and IC5; this both clocks the main address counter (IC10 in fig. 2a) and, via the Schmitt trigger IC7, provides a variable-width

trigger IC7, provides a variable-width gate pulse.
In spite of the six adjustment points

Ipotentiometers P1...P6], the circuit can be set up fairly simply, without the need for any special measuring equipment. The circuit is adjusted correctly when a change in the 'e' input from '0' to '1' causes the voltage at output A to increase by 1 V. This voltage can be adjusted by means of P3. P2 should be set such that the output voltage changes by 0.5 V when inputs 'b' and 'q' on high.

Fine tuning is performed by means of PI. A change in state of input 'a' should correspond to a change of 1/12 V in the output signal. PS should be adjusted such that the output fraquency doubles when input 'g' goes high. PA is used to compensate the offset voltages of ICA and ICS, Finally, P6 determines the width of the gate pulse.



chain

basic computer Elektor 49, Mey '79, p. 5-34, The circuit diagram (figure 3) contains several minor errors. The pinning of ICB should be as follows: D-C-B-A along the top should be pin numbers 5, 4, 3 and 2 respectively; along the bottom the pins ere 10, 11, 12 and 13. Gates N1 ... N4 ere ANDs, not NANDs: the output of N1 is point 27c, that of N2 is 31s and that of N3 is 31c. Finally, the 'X' and 'Y' indications to the left of IC1 are transposed. As far as these points are concerned, the printed circuit

board is correct. Of greater consequence is the fect that two versions of the NIBL-ROM exist (IC10 in figure 7), In some cases, the chip select pins 120 and 21) must be connected to positive supply, as shown; in others, however, they must be connected to supply common! This can be achieved quite easily, by removing the wire link connecting these pins to pin 24; e new wire link to connector pins 32s and 32c can then be ended Finally, it was perhaps not made sufficiently clear that the Basic microcomputer card uses connector pins 32a and 32c for supply common, wheress the 4K RAM card uses pins 4a,c and 16a,c. A wire link on the SUS board connector card is therefore required.

elekdoorbell

Elektor 50, June '79, p. 6-12. The numbering of the syntches as used in the text does not correspond to that used in the circuit and on the p.c. board. The simplest solution w to correct the text numbering. as follows: \$1 (text) becomes \$11 (circuit); \$2eb = \$10eb; \$3 = \$9; S4 = S1; S5 . . . S11 = S2 . S8. The CE input of ICS, referred to in the text, is pin 13.

On the p.c. board, two minor modifications may sometimes prove nacessary: pin 11 of IC7 should be connected to supply common (i.e. pin 12), and pin 14 may be connected to pin 13 instead of to positive supply. Note that if the specified RCA type CD 4034B is used, the letter modification is unnecessary ton 14 can be left as it is), but for some other semi-equivalents (motably the Motorola 14034BCP) www.usential.

aquarium thermostat

Elektor 50, June 79, p. 6-29. In the circuit diagram, OB is shown connected between pins 11 and 72 of IC3, This diade should in fact be connected between pin 11 of IC3 and the +12 V line: orn 12 of IC3 is connected only to D7. in other words, these two diodes are connected in the same way as O11 and O12, further down the

July/August 1979

Circuit 25: lines r thermometer In the circuit diagram, the indications 'IC1' and 'IC2' are trans-

Circuit 27: moisture sensor The sensor should be connected

in perallel with R1, not in series with R2. Circuit 30: automatic heated rear

windscreen To evoid confusion: pin 3 of IC6 is the clock input; it is indeed connected to supply common, as shown

Circuit E: servo emplifier The printed circuit board is reproduced at twice the actual size; the actual size is shown below.





function generator IC1 and IC2 should be type 2101, not 2102 Circuit 90: uP-programmable

spesd controller for model reil-WEVS In figure 1, the output pinning of

IC2 is Incorrect; from too to bottom, the pin numbers should resd: 7 (=Q1), 6, 5, 4, 9, 10, 11 (=07). In figure 3, the supply voltage should be 5 V. Circuit 100: 256-note sequencer

In figure 1e, pins 4 of IC1 . . . IC3 should, of course, be connected to -15 V. In figure 1c, e 1 n capacitor is shown between pin 3 of N38 and supply common. This capacitor should be connected between pin 4 of N24 and supply common

Circuit 106: charosynth In figure 2, the connections to the left-hend keys should ell be moved one position to the right. The first key is thus connected to the R1/R2 junction. In figure 3. R95 (between T10 and A3) is shown connected to +15 V; it should, however, be connected between the base of T10 and the inverting input of A3.

Circuit 102: video pattern generazor

Pin 12 of N16 is shown connected vis a diode to pin 7 of IC3b; (t should, however, connect to pin 6. Furthermore, R28 is shown connected to the right-hand side of the Xtal, whereas it should be connected to the top of C1. The author has suggested two improvements to his circuit: the

resistor values for R38...R45 can be decreased by a fector of 10 (e.g. 47 k instead of 470 k). end a diode may be added between the output of N4 (cathode) end pin 13 of N12 (anode).



Long range photoelectric switch

The E3N-30 Photoelectric Switch from IMO Precision Controls has an operating range of 30 metres. The E3N-30 incorporates the letest innovations in design and circultry including the unique 81-COLOUR indicator to speed setting up time and indicate the stable operating range by colour, red for unstable, green for stable The E3N range, which includes Oiffused Reflection and Regular Reflection types, has a tough discast casing to protection class IP65. The infre red LEO light source ensures long operating life and high immunity to embient light. Transmitter and receiver are compact units measuring only

power switching transistors designed to meet stringent execufications on temperature and hermeticity for operation in harsh environments. The transistors, evailable for 10 A and 15 A potration, are high-voltage NPNtypes designed for use in offline supplies and other high-voltage switching applications, and are 100% tested at high temperatures for 100°C parameters. These transistors, types 2N6674-78 and 2N6689-93, feature high voltage capability, with collector-emitter voltage ratings of 350-450 V, high switching spesds, low saturation voltages and high safe-operatingratings - cheracteristics which make the devices particutarly suited to use in offline switch-mode power supplies, convertor circuits and pulse-widthmoduleted reguletors. An importent feeture of the SwitchMex transistors in the 100% testing for parameters that are critical in the design of high-power switching circuits, such as switching times (including inductive turn-off time)



90.5 mm x 40 mm x 40 mm with simple terminal connection via conduit entry. Available in opersting voltages from 12 V DC with s voltage output or 24 V OC

with a power output capable of switching up to 200 mA. 110/ 240 V AC operation is also available via the S3N Control Unit. IMO Precision Controls Limited, 349 Edgware Road.

London W2 1BS. Tel.: 01-723 2231/4 or 01-4027333/6

(1293 M)

RCA Solid State - Europe. Sunbury-on-Themes.



Middlesex, TW16 7HW, (1283 M)

and saturation voltages. These are

tested at 100°C as well as 25°C to

provide the information required

The RCA SwitchMex Types

2N6674-78 are supplied in stes!

JE OEC TO-20 MA (TO-3) her-

metic peckages, and the 2N6689

93 are supolied in the JEOEC

TO-211 MA (TO-61) package

with a steel harmetic shall, a solid

copper header/stud for low ther-

mal resistance, and all terminals

electrically isoleted from the

for worst-case design.

Switching transistors designed for harsh environments

RCA Solid State has introduced two new ranges of SwitchMax





Miniature LCD panel clocks

Ambit ere now stocking a miniature panel clock, that provides all usual timekeeping functions in both UK and US formats for time, day, date,



The unit is quartz controlled (with access to the trimmer for fine edjustment), and includes en incendescent becklight feeture. An alarm function is available to drive a bleeper or some other external means of indication. With a running consumption of only 6 µA, the PCIM161A is suited to a variety of applications - renging from all types of consumer electronic equipment, to instrumentation, telephones, communications equipment etc. The unit requires only three mamentery contect switches for setting etc and its accuracy is within ± 2.5 minutes per year. Ambit Internstions! 2 Gresham Road.

(1280 M)

Brentwood, Essex,

Telephone: (0277) 227050.

New product range catalogue from Marshall's

Marshall's announce the publishing of their new 1979/1980 product range catalogue on October 12th

This edition contains many new products within it's 60 pages, including an increased range of IC's, micro-power LCD clock modules, deta and educational backs etc etc.

At the same time Mershall's ere lounching their new 'budget' credit card scheme, in conjunction with RETRA. This will enable customers to purchase goods on credit from any of the four Marshall's retail branches Minimum monthly repryment is £ 5.00 and goods 20 times this

may be purchesed. Further details from Marshall's branches efter October 12th 1979. Another significant point is that Mershall's have reduced prices on their top line products, resulting in very competitive prices

Twin reply peid order forms are supplied in each catelogue to facilitate easy ordering and faster turn round on supply The cetelogue costs 50 p from eny Mershall's branch or 65 p post paid from their head office

Marshall's (Head Office). Kingsonte House, Kingsgate Place. London NW6 4TA

(1294 M)

Four-colour plotter

Tel.: 01-624 0805.

An assy-to-use 11 by 17 in. (A3 size) microprocessor-controlled platter that produces low-cost, high-quality multicolour graphic plots with date sent from virtually any computer or controller has been introduced by Hewlett-Packerd. Interface is vie RS 232/V24 esynchronous seriel ASCII at eny of eight switch selecteble boud retas from 75 to 2400. Special design features also enable the plotter to be coupled into en existing computer terminal RS-232/V24 inter-

face The new 7220A four-colour plotter generates cheracter sets, rieshed lines, and implements scaling and other high-level functions internally. Plotting colours are selected and changed under program control to produce high resolution graphic plots and overhead transparencies. There ere seven colours evailable for clear film plotting

Cheracter plotting speed of over two cheracters per second allows fully annotated graphs to be produced in minutes. A buffer with over 1100 bytes has been incorporated to store incoming graphic plot deta so that 1/0 interrupts and date communications between computer and plotter era minimised. As an option, an additional 2048 bytes of buffer storage can be made

augilable The plotter's built-in language contains two categories of instructions: device control and graphic instructions. The graphic instructions comprise more than 45 two-letter mnemonic instructions from the Hewlett-Packard Graphics Language (HP-GL) which equips the plotter with such capabilities as relative end ebsolute plotting, point digitising. labeling, character sizing, integer

scaling and window plotting. No specialised programming experience is needed to use the new pintrer

For applications requiring unattended operation, the 's' version of the new plotter features automatic page advance, an internal paper supply and paper cutter, end e detached paper tray to collect full or half-page plots. Hewlatt-Packard Ltd, King Street Lane, Winnersh. Wokingham, Barkshire RG11 5AR

(1286 M)

Single knob measuring bridge from Siemens

Siemens Ltd is marketing a single knob resistence bridge that can be operated by one hand - a feature that greatly facilitates simultaneous note-taking. The bridge is available in two types: model M273-A1 comprising e Kelvin double bridge for meesuring low resistance values (200 u-ohms to 2200 milli-ohms) and model M273-A2 with a Wheatstone bridge for medium resistence values. The low resistance model has built-in measuring lead compensation.



The bridge is balenced by an easy-to-read galvanometer read against a deviation scale, Both types are accurate to +/- 1% of the measured value (+/- 1.5% of the lowest range of model M273-A1) end can withstend a 2 kV voltage surge. The power source is two stendard IEC R14 1.5 V cells. Alternatively, 2 or 6 V d.c. externel power sources can be used which, generally, increase the reading accuracy. Both models are in a rugged moulded plestic housing A leather case is avertable (extra) for heavy-duty use. Typical dimensions ere 112 mm (4.4in) wide x 84 mm (3.3in) deep x 192 mm (7.5in) long. The weight is 1.1 kg (2.41b).

Siemens Lumrted. Siemens House, Windmill Road, STIMBURY OF THAMES Middlesex, TW16 7HS. Tel: (09327) 85691.

High quality transient signal processors

Bryans Southern Instruments Limited of Mitchem, Surrey, heve just announced the Introduction of a new range of high-samplingfrequency, high-resolution trensignt signal processors. Priced to sust modest laboratory budgets, these new units are known as the Series 523A.

They offer a 10-bit resolution (i.e. 1 pert in 1024), at the high sempling rate of 10 MHz, so that the shortest sampling interval is 100 nanoseconds



When switched to dual timebese mode, the first pert of the recording is recorded at timebase rate A, and the second part at rete B. The point at which the change is made, is set-up by the user on a two-digit thumbwheel switch. It is calibrated in multiples of sweep time, with a resolution of 0,05 from 0 to 0.95 of

the sweep time. These dual timebase facilities can be used even when pretriggering is in operation - a unique feature for this type of instrument. Therefore, one can relerence e short event of just a few microseconds during a trigger condition, many seconds in advance of a fast signal and stiff record the pre-trigger information. At the same time, the 523A mainteins an exceptionnelly high resolution of the time

and emplitude of the signal. These trensient signal processors are evailable in single- or dualchannel versions, each with 4096word memories They cen be interfaced to many peripherels and computers by RS232C. IEEE488/1975 (G.P.I B.), or the general purpose interface board. If required, up to seven instruments can be bussed together for digital output purposes

Bryans Southern Instruments Ltd. Willow I are Mitcham, Surrey, CR4 4UL,

Tht.: 01-640 3490

(1288 M)



(1279 M)

market

New, miniature, low-cost temperature recording spots

The temperature responsive triangle turns irreversible black from original white after having been exposed to its rated temperature for fractions of a second. Such single temperature spots, or multiple temperature squenced stripe



can record the maximum temperature level of any surface to which they have been affixed over the antire application history with an accuracy of ± 1% the price per sort can be as lower 2 peace.

Cobonic Ltd., Knepton Mews, Seely Road, London SW17 9RL,

Tel.: 01-6724150.



High power servo amplifier end motor driver.

or

í.,

The new SH3015 high power amplifier from Fetrchild has been developed for applications requiring high current and high voltage capability. It is able supply up to 5 A continuously into a load between ±35V. Notable fetures include immenal

compensation, programmable current limiting and excellent stablity when driving into resistive

and inductive loads.

The amplifier front-end incorporate a µA 741 operational amplifier with deditional votage and current gain stopes so enabling it to mact the performance required for serve systems. The output is protected from votages transients caused by inductive surges. Output current limit is salected by placing appropriate resistance between the supply plan and the respective current limit bins. The case is electrically bins. The case is electrically

Absolute maximum retings include an internal DC power distipation of 70 W with a case temperature of 25°C, input voltage differential 30 V and DC output current of 10 A.

Fairchild,

isolated.

Camera & Instrument (UK) Ltd., 230 High Street, Potters Ber, Harts EN6 5BU, Telephone: (0707) 51111

(1231 M)



Miniature float switch for liquid-level sensing

The second secon

Maximum contect rating for the Hamilin P219 is 10 W, at it can switch voltages of up to 500 V. Hamilin Electronics Europe Ltd., Diss.

Norfolk IP22 3AY, Tel.: (0379) 4411/2/3.

(1295 M)



market

Switching regulator power supplies

Now svellable from Amplicon Electronics Limited are four edditional models to their existing range of switching power supplies. These new models, designated RT153, RT154, RT303 and RT304, are designed to meet increasing micro processor applications.

They employ isoleted auxilliary outputs of 5 V and 12 V or 5 V and 15 V in addition to the main 5 V output.

RT153 -- 5 V @ 30 emps 12 V @ 5 amps 5 V @ 2 emps RT154 -- 5 V @ 30 emps

15 V @ 4 ampe 5 V @ 2 emps RT303 — 5 V @ 80 emps 12 V @ 5 emps

5 V @ 5 emps 5 V @ 5 emps 15 V @ 60 emps 15 V @ 4 empe 5 V @ 5 emps

The RT153 and 154 models are packaged in the standard 5 x 5% x 9% (T15) case size and the RT303 and RT304 are in the standard 5 x 8 x 10 (T30) case size, with combined total power retings of 150 watts and 300 watts respect.

ively.

Amplican Electronics Ltd.,
Lian Mews,

Hove BN3 5RA, Tel.: Brighton (0273) 720716.

(1292 M)

marke

SEA COM — a new 'do-it-yourself' intercom for yachts A new 'do-it-yoursell' talk-back

A new contryoursell talk-back system for the private yachtsman has recently been introduced by Barkway Electronics. Sea Com is a low cost, point-to-

point intercom/loudneller system which is as simple to install as a car radio and is being sold in 'do-it-yoursell' kits comprising a master unit and two speakers. Barkway claim Sas Com is the only system of its kind only system of its kind on the market and anvisage good sales throughout the world. High quality sound and water-

proof equipment guarantee commands and answers will be heard correctly, even in the worst possible conditions and Sea Comalso features an alerm werning tone to alert other shipping in bad visibility.

The sub units can be fitted in the fore and aft positions of the boat, increasing solery at sea not only through clear sound but by cutting down the amount of movement necessary on board in person to person exchanges.



The system is designed for continuous operation and can be left on in the standby position for monitoring from lookout positions in bad visibility.

The See Com control, or master unit consists of a heavy duty watertight aluminium case coated in Rilisen nylon and the system fitted with high output loud-speakers, hand microphone, volume control, speaker selector switch and tone alert button. The equipment has a power

The equipment has a power output of 10 watts and can operate on 12 or 24 volts O.C. from the ship's batteries.

Barkway Electronics Limited, Barkway, Royston, Hertfordshire SG8 BEE England. Telephone: Barkway

(0763 84) 666

(1282 M)



Wire twisting plier

The Milber Safety Twist wire twisting plier is a versatile tool that will handle wire looking of nuts, bolts, screws and caps.



together with twisting wires and coals in electrical and strip the wire to be twisted and stilling levels to be wire to be twisted and stilling levels where it twisted amply by pull-race spiral knob. The piler on ball-race spiral knob. The piler has an overall langth of 10% political spiral knob. The piler has an overall langth of 10% piler in langth of 10% political and the piler in the

Toolrange Ltd., Upton Road, Reading RG3 4JA, Tel.: (0734) 29446 or 22245.

(1291 M)

Gould Advance OS 3500 60 MHz oscilloscope

Gould Instruments Division has lounched a new 60 MHz dualtreca ganeral-purpose oscilloscope, the Gould Advance OS 3500, featuring a wide range of measurement facilities normally found only on higher-bandwidth instruments. Among the special features of the oscilloscope are comprehensive triggering facilities with a trigger bandwidth of DC to 100 MHz. and an optional add-on digital measuring unit for accurate measurements of emplitude, time

and frequency. The Gould Advance OS 3500 nsellinscome uses en 8 cm x 10 cm high-writing-speed cathoda-ray tuba with an accelerating potential of 12 kV to give a bright, easy-toread display. The instrument is designed for portability; meesuring 32.5 cm wide x 18 cm high x 46.5 cm deep, and weighs 10 kg, and the carrying handle elso functions as a fully adjustable stand.

The Instrument has two input chennels, Y1 and Y2, which provide meximum sensitivities of 2 mV/cm over the full 60 MHz bendwidth, and a special control circuit is incorporated to nullify thermal drift.

The wide range of operating modes aveilable on the OS 3500 includes comprehensive delayed timebase and triggering facilities. Vernier control of sweep daley time allows accurate timing measurements to be made, and the delayed timebase can be started by the mein timebase swaap or triggered elter a preset sweep delay. The main and detayed timedase controls are completely separete

For the study of complex weveforms, on elternate timebase sweep mode is incorporated, which allows the main timedese

(intensified) and delayed time base sweeps to be displayed simultaneously. This mode is selected by a single pushbutton, and can be used with single or dual-channel operation. The advantage of this mode is that an immediate relationship is established between the main timebase signal and the detail being swept by the delayed timebase, and changes in the settings of either timebase do not involve the operator in any further edjustments.

Among the comprehensive trigger facilities is a triggerview function. activated by a single pushbutton, which allows continuous display of the signal triggering the main timedasa, whether the source is internal or external When the instrument is operated in the dualchannel and trigger-view modes, three traces are displayed, and this facility simplifies the procedure of setting the trigger level for single-event signels as well as establishing the presence of a trigger signel under difficult massuring conditions. For measurements on a circuit with Its own system clack, the oscilloscope can display and be triggered from this signal, while the two main input channels remain free to study other important informetion

Another feature which simplifies the triggering of complex weveforms is variable trigger hold-off, which can be continuously edjusted up to approximately one sweep length of the mein timebase on most ranges.

Gould Instruments Division, Rosbuck Road, Hainsult, Essex 1G6 3UE. Telephone: 01-500 1000



Add-on digital measuring

The new Gould Advance DM3010 digital measuring unit from Gould Instruments Division is designed to increase the basic accuracy of the OS3500 dual-trace 60 MHz oscilloscope in the measurement of amplitudes and time relationships. Offered as a fectory- or service-fitted option to the OS3500, the unit provides a 3%digit digital-voltmater facility via e separate floating input, as well as increased voltage and time accuracies when switched to operate with the oscilloscope. For time measurements, a second

'bright-up' section of the oscilloscope's main timebase sweep is introduced and controlled from the DM3010. The period between the first end second bright-up sections is eccurately displayed on the instrument's light-emittingdiode display For emplitude messurements, a second complete sweep of the channel 2 signal is introduced, and the bottom of this signel is adjusted to coincide with the top of the besic display (1221 M) to provide an accurate digital readout

Operated es en independent digital voltmeter with the saperate floating input, the DM3010 measures voltages from 200 mV to 1000 V DC, with e resolution of 100 aV and an accuracy of ± 0,15% of reading ± one digit. Resistance and current can also be messured. The combined accu racy of the DM3010 and OS3500 is ± 1% of reading ± two digits for time and ± 2% of reading ± two digits for emplitude measurements up to 5 MHz. Above 5 MHz, the accuracy is conditioned by the vertical amplifier roll-off to -3 dB at 60 MHz.

The additional eccuracy offered by the DM3010 is of particular use in applications such as the measurament of digital-circuit time relationships, including memory timing and propesstion deleys. Phase and risetime measurements can also be made more precisely.

Gould Instruments Division Roebuck Road, Hainsuit From 1G6 3UF



Low-cost keyboard subsystem

Electronic Brokers' new low-cost Model 771 ASCII Keyboard is especially suited for use with the letest inexpensive video terminal and display boards.

The combination of the 771 keyboard subsystem, and a video terminal board mounted in the user's meinframe, provides en ettractive and versatile cost-saving alternative to conventional onepiece CRT terminals. Compect, reliable, and rugged, the 771 Keyboard is ideal for use in small business, word processing, or softwere development applications for personal, business, scientific or educational microprocessor systams

Standard features include full ASCII alphanumeric section; convenient current control and numeric ped, two-key rollover for low error rate, Upper & lower case plus control codes; TTY mode for upper-case only operation; Timed autorepeat on all keys; all modes stendard perellel interface; detechable industry standard connector, non-glare keycaps; robust steel desktop englosure

The 771 Keyboard is supplied fully essembled and testad, with complete documentation, requiring only power and data connections to the user's system for operation. Supplied mounted in en all-steel desktop enclosure. finished in textured ISM blue and black this Keyboard is a perfect complement to modern microprocessor hardwere.

The KB771 is priced at a modest £ 95.00, with discounts for quan-

Electronic Brokers Limited, 49/53 Pancres Road, London NWI 2QB. Telephone No: 01-837-7781.



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